FIG.1

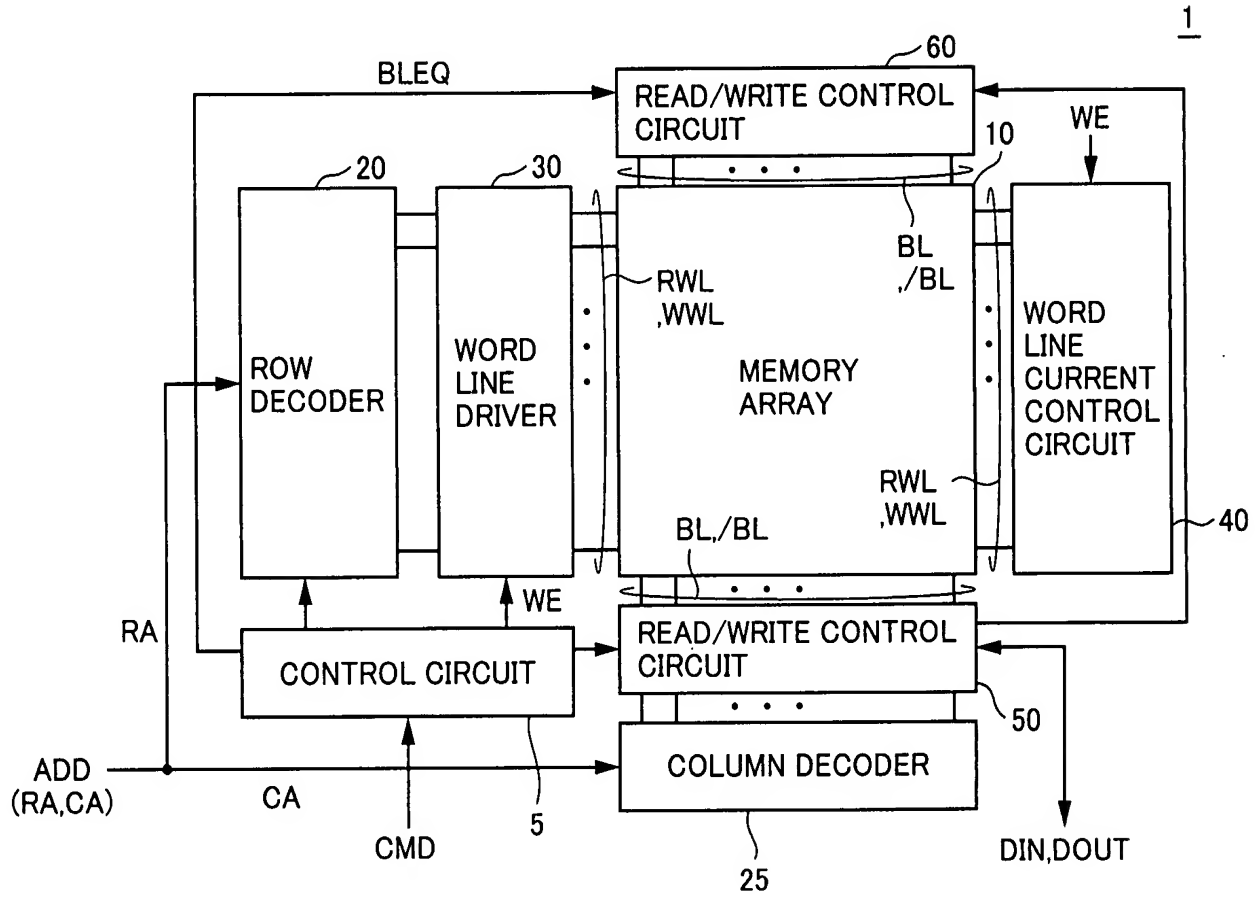
1
60
BLEQ
READ/WRITE CONTROL CIRCUIT
WE
10
20
30
BL
,/BL
RWL
,WWL
ROW DECODER
WORD LINE DRIVER
MEMORY ARRAY
WORD LINE CURRENT CONTROL CIRCUIT
RWL
,WWL
40
BL,/BL
WE
RA
CONTROL CIRCUIT
READ/WRITE CONTROL CIRCUIT
50
ADD
(RA,CA)
CA
COLUMN DECODER
CMD
5
25
DIN,DOUT

FIG.2

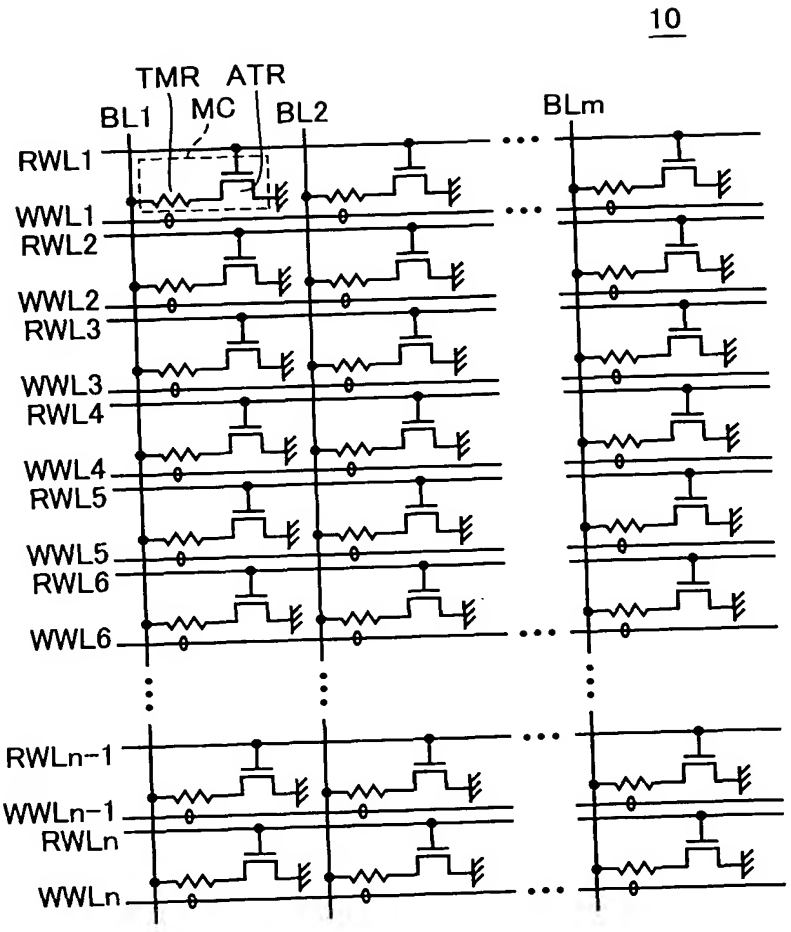
10
TMR
ATR
MC
BL1
BL2
BLm
RWL1
WWL1
RWL2
WWL2
RWL3
WWL3
RWL4
WWL4
RWL5
WWL5
RWL6
WWL6
RWLn-1
WWLn-1
RWLn
WWLn

FIG.3

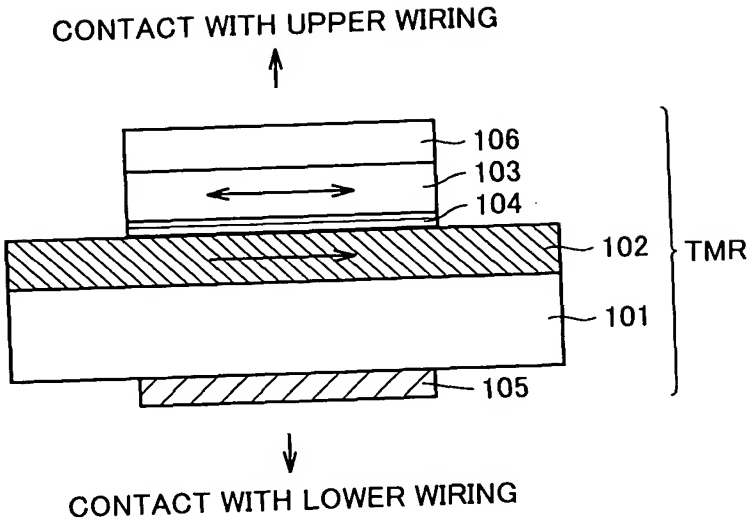

FIG.4

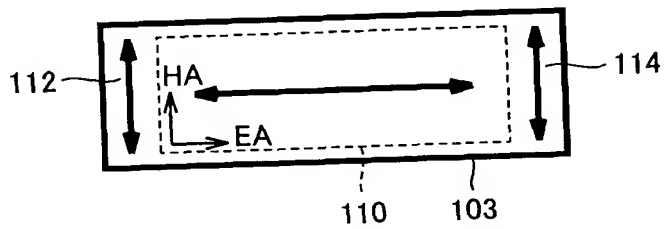

FIG.5

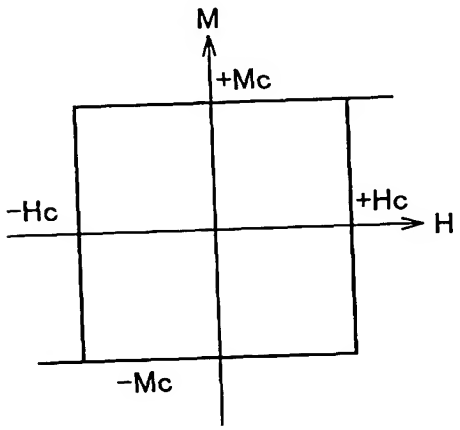

FIG.6

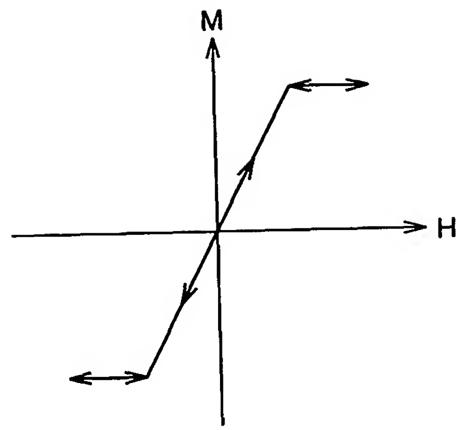

FIG.7

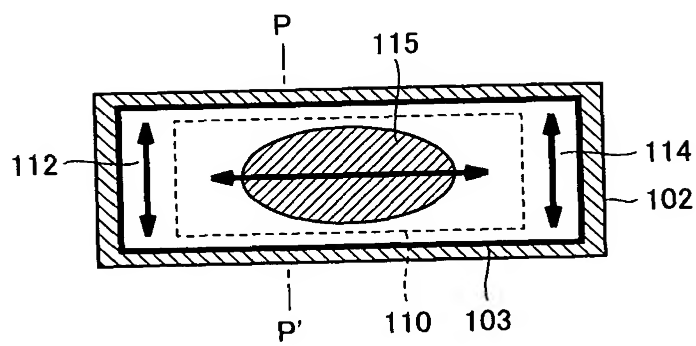

FIG.8

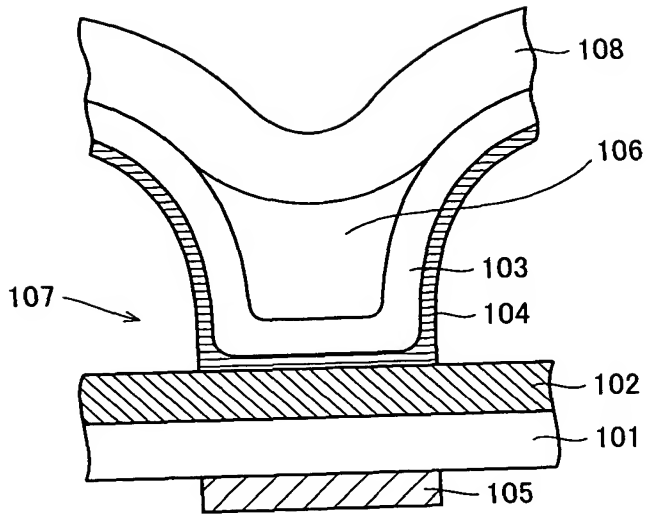

FIG.9

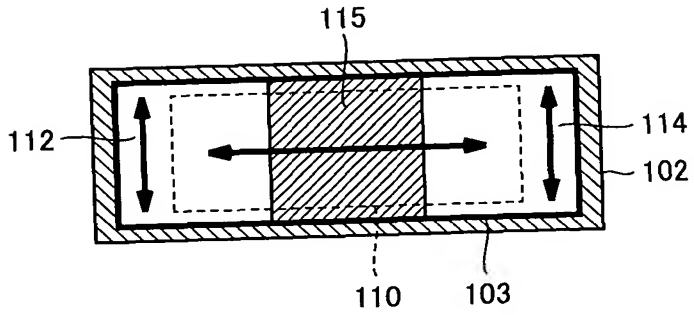

FIG.10

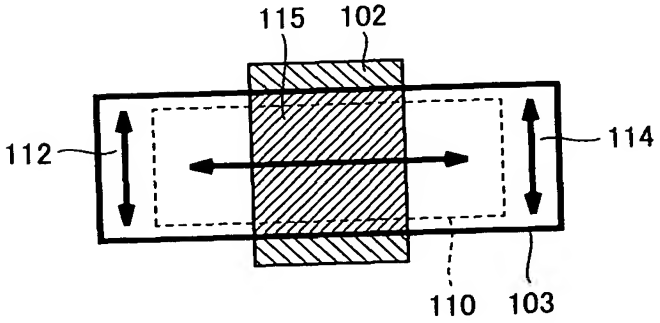

FIG.11

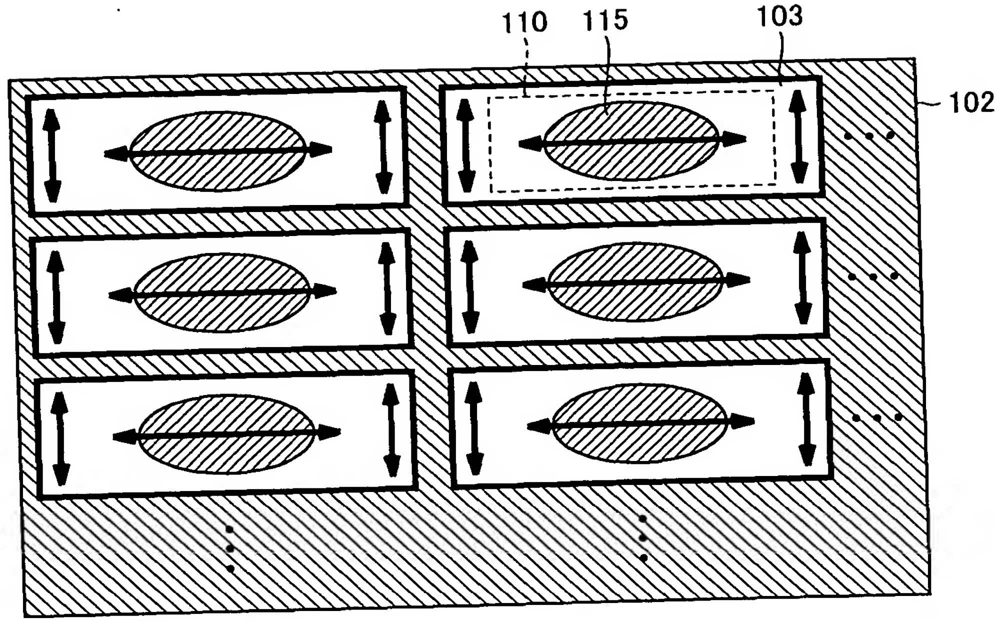

FIG.12

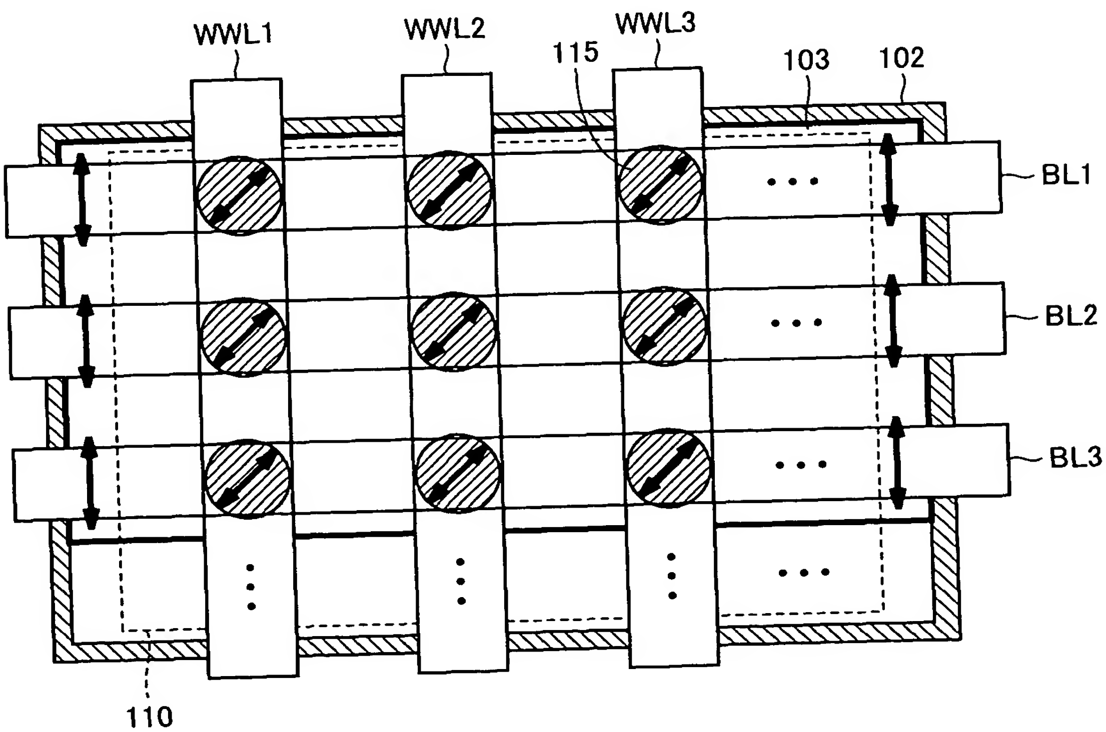

FIG.13

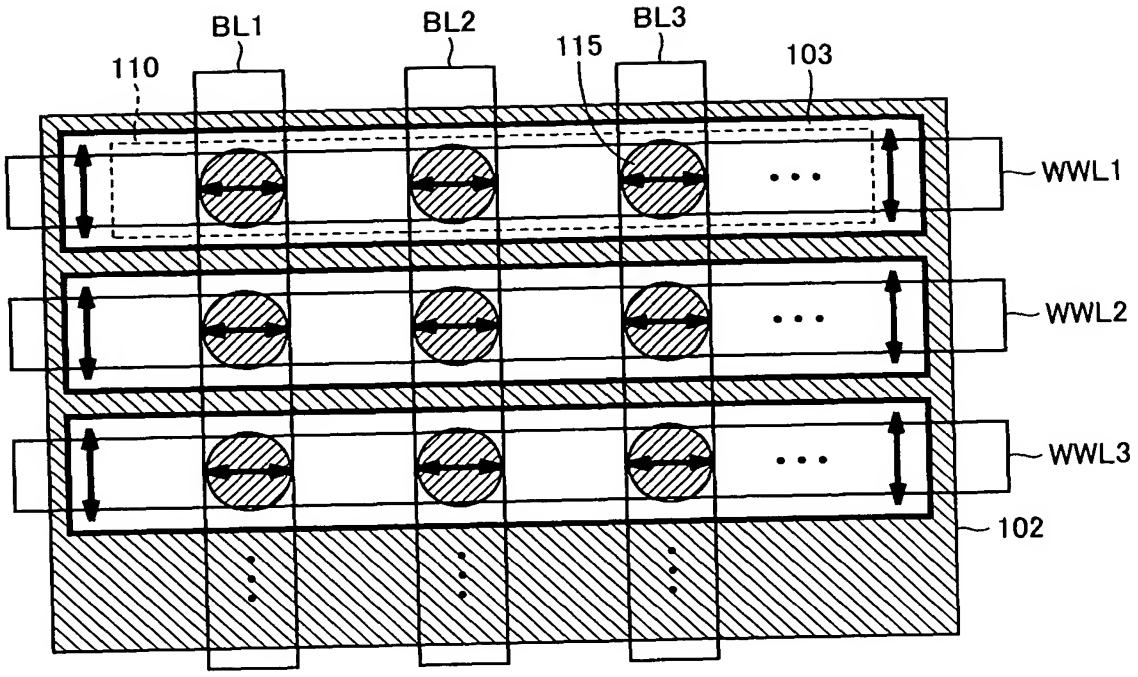

FIG.14

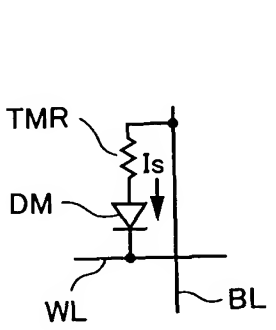

FIG.15

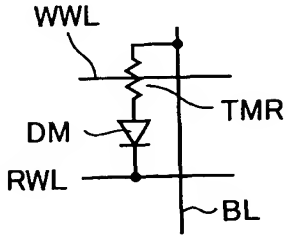

FIG.16

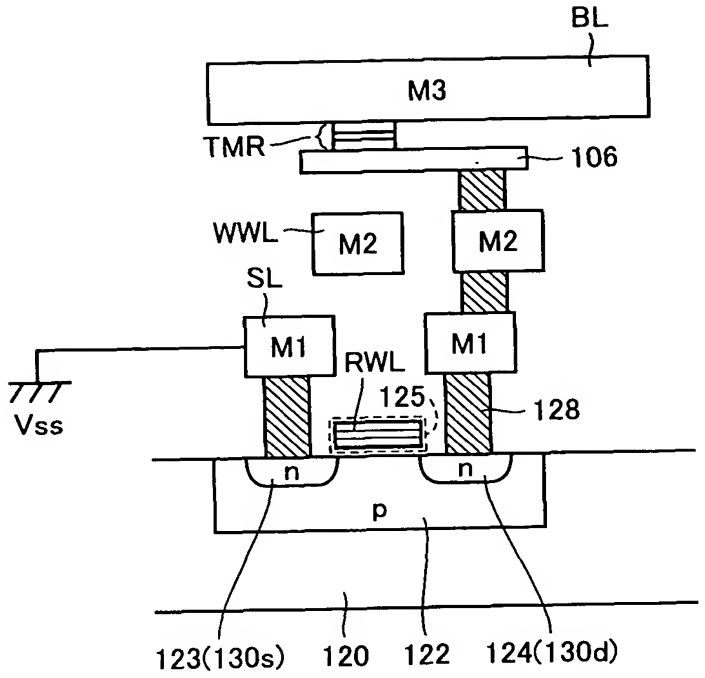
BL
M3
TMR
106
WWL
M2
M2
SL
M1
RWL
M1
125
128
Vss
n
n
p
123(130s)
120
122
124(130d)

FIG.17

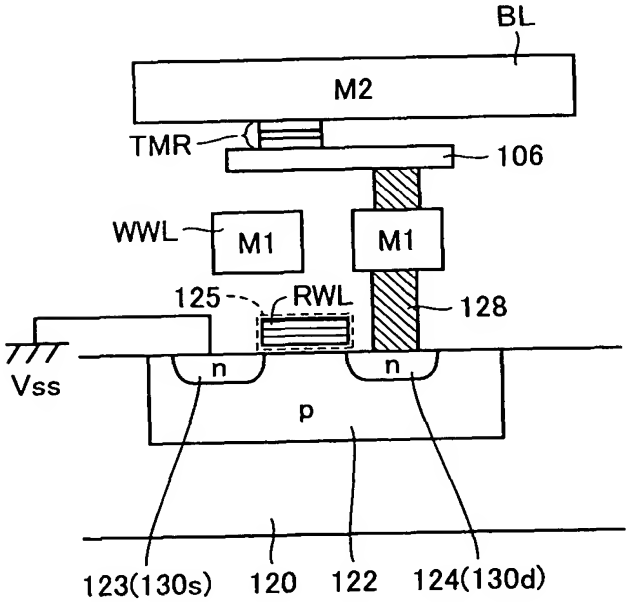
BL
M2
TMR
106
WWL
M1
M1
125
RWL
128
Vss
n
n
p
123(130s)
120
122
124(130d)

FIG.18

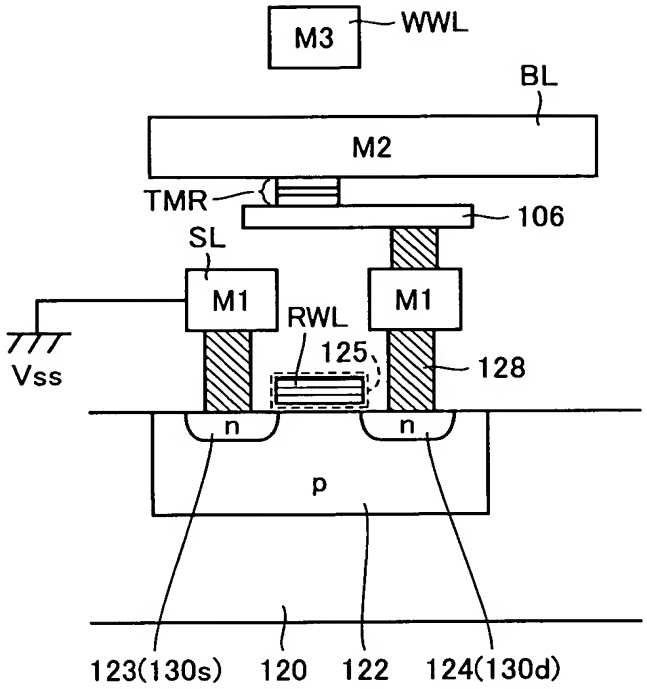
M3
WWL
BL
M2
TMR
106
SL
M1
M1
RWL
125
128
Vss
n
n
p
123(130s)
120
122
124(130d)

FIG.19

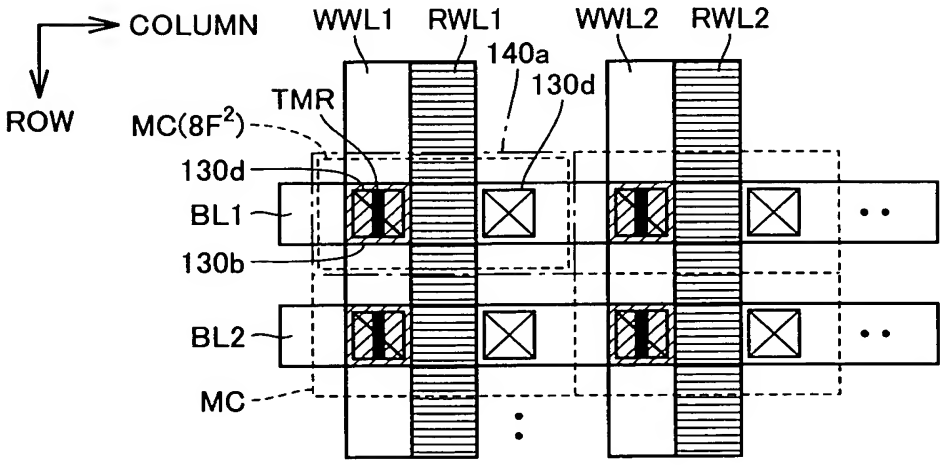
COLUMN
ROW
WWL1
RWL1
WWL2
RWL2
140a
130d
TMR
MC(8F²)
130d
BL1
130b
BL2
MC

FIG.20

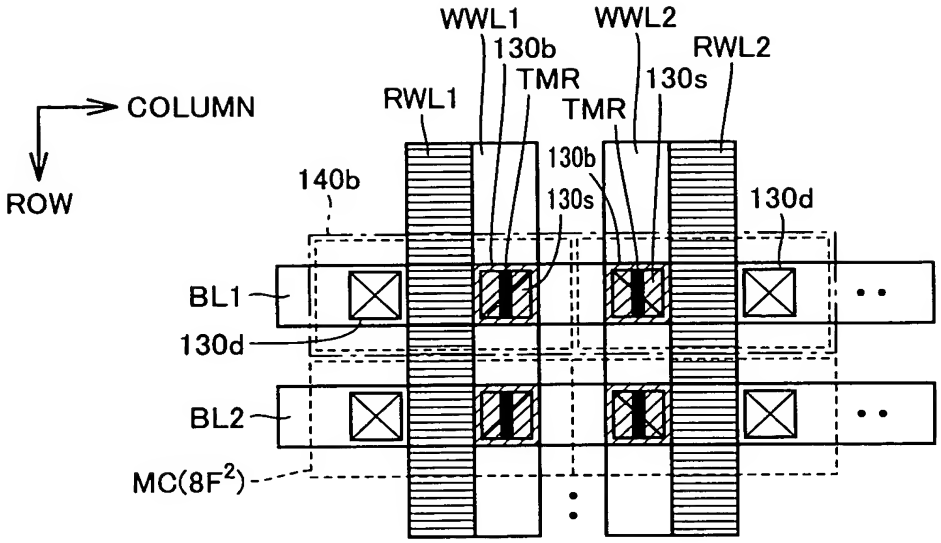
WWL1
WWL2
130b
RWL2
TMR
130s
RWL1
TMR
COLUMN
ROW
130b
140b
130s
130d
BL1
130d
BL2
MC(8F2)

FIG.21

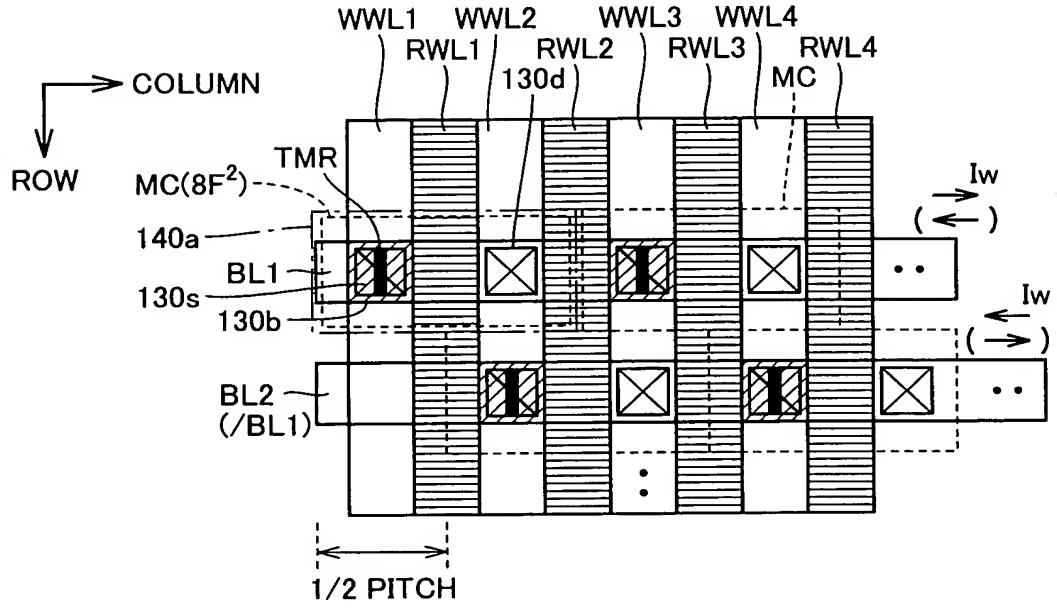
WWL1
WWL2
WWL3
WWL4
RWL1
RWL2
RWL3
RWL4
130d
MC
COLUMN
ROW
TMR
MC(8F2)
Iw
140a
BL1
130s
130b
Iw
BL2
(/BL1)
1/2 PITCH

FIG.22

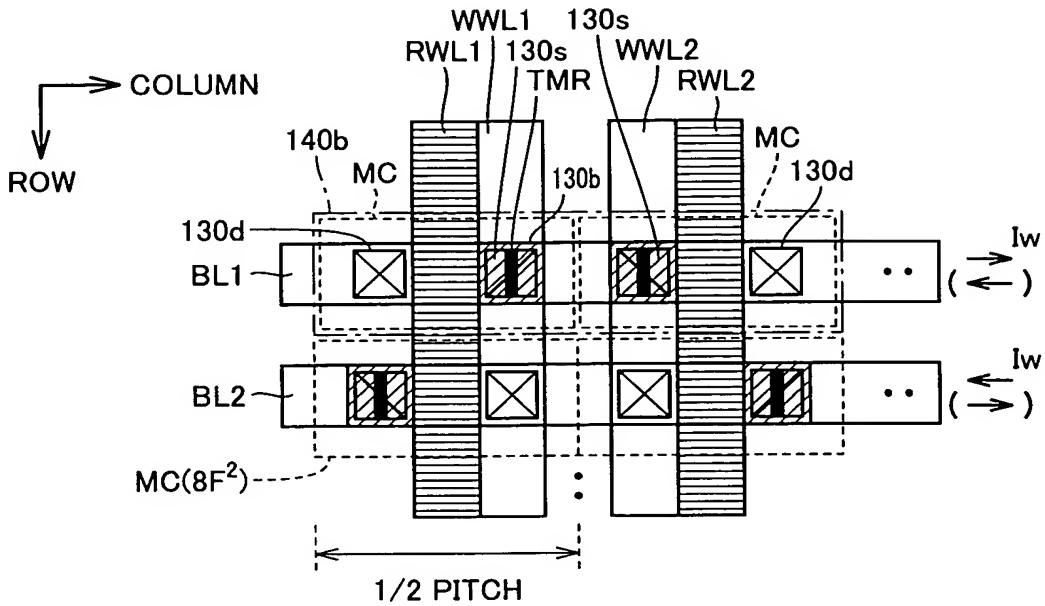

FIG.23

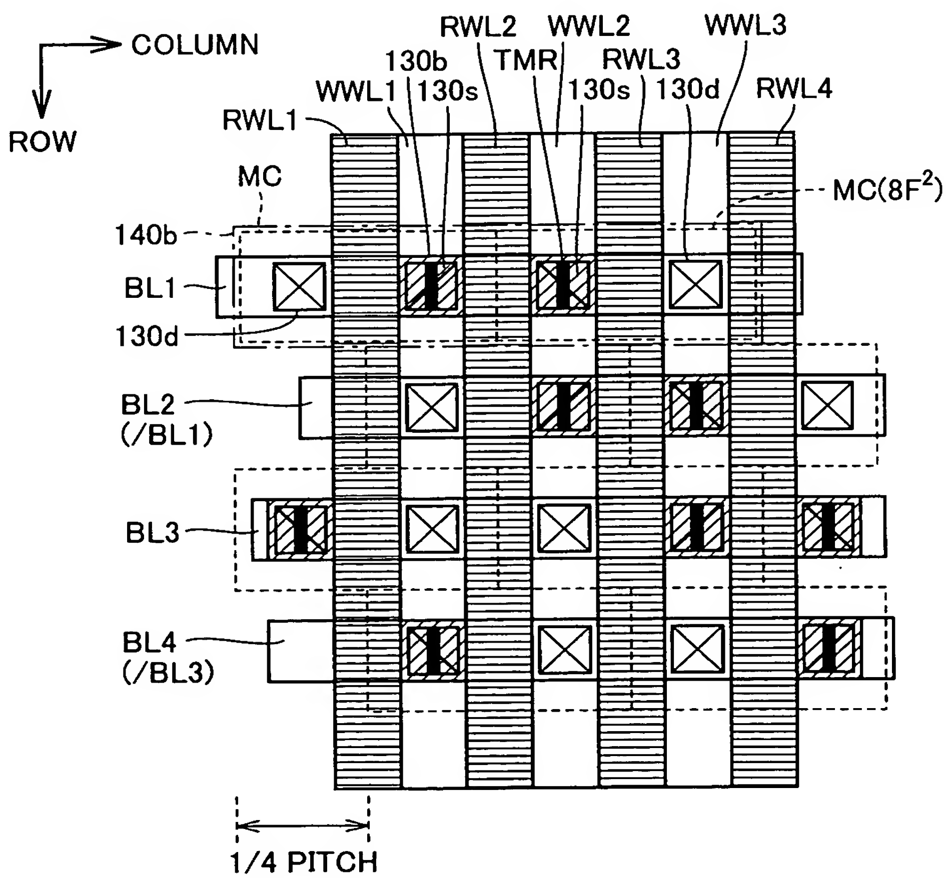

FIG.24

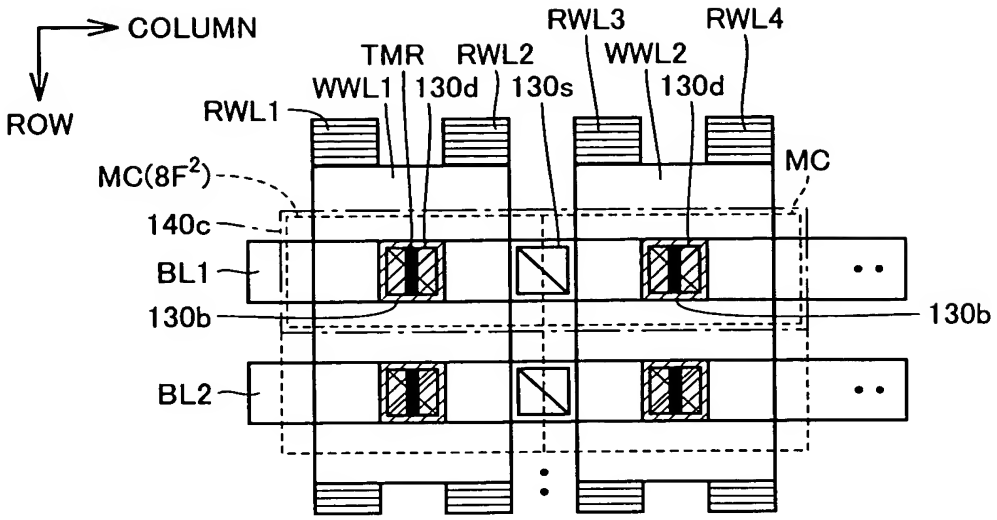

FIG.25

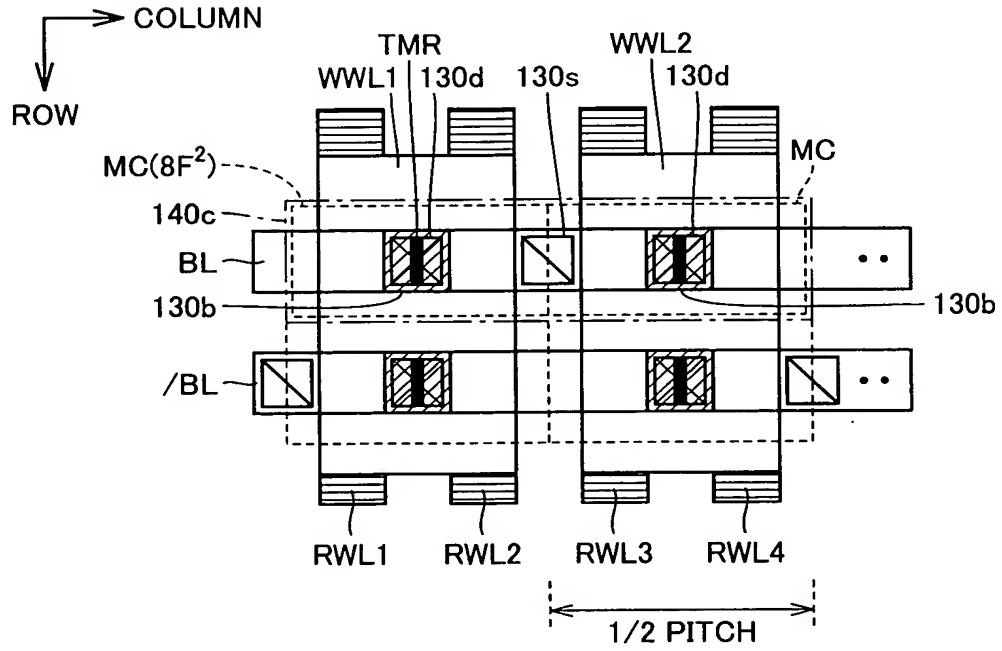

FIG.26

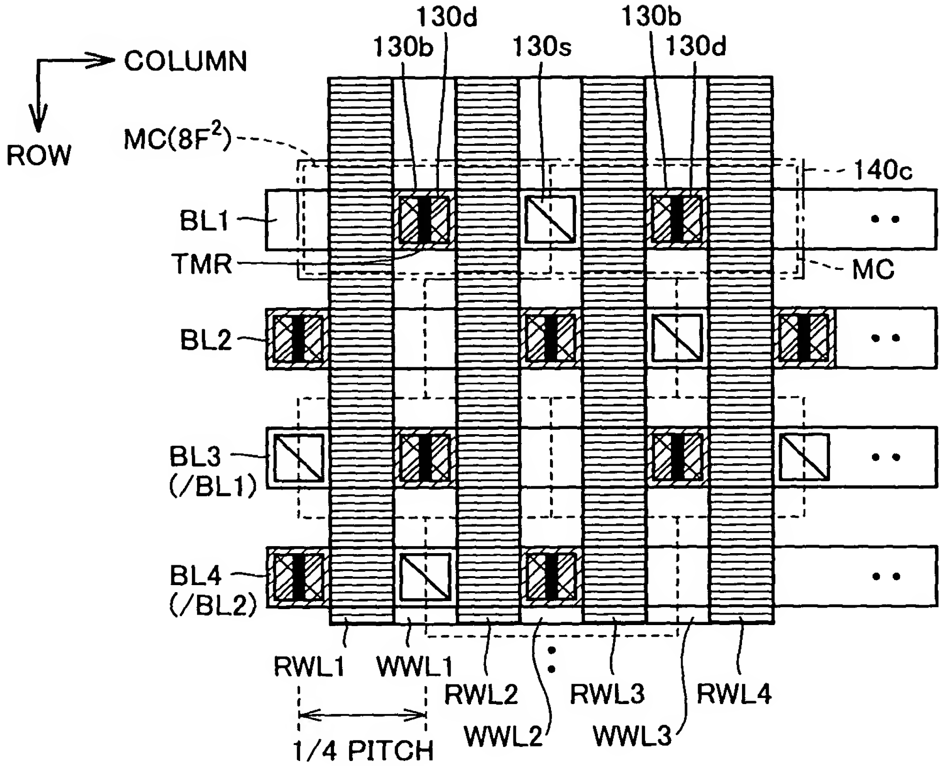

FIG.27

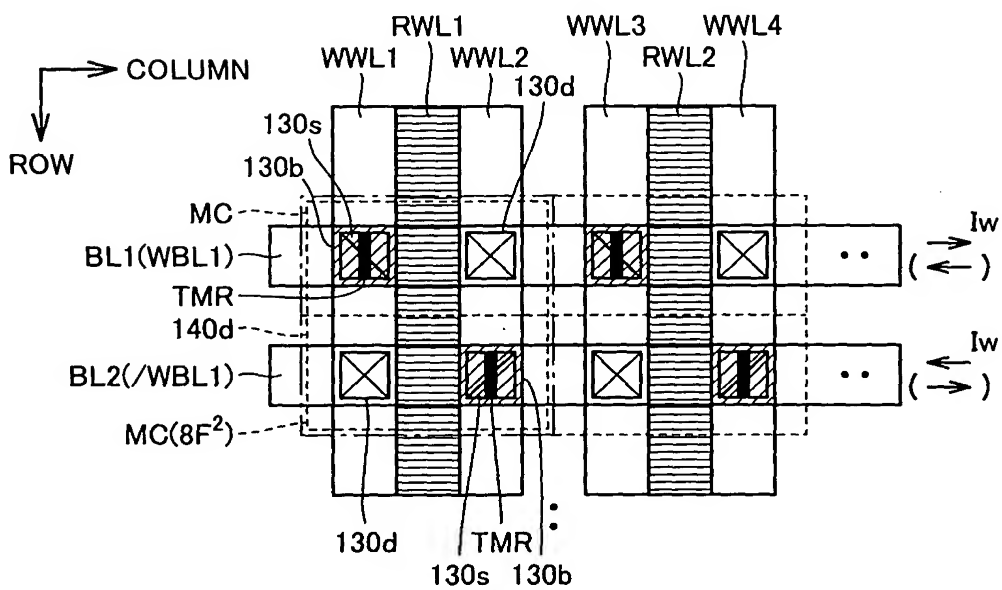

FIG.28

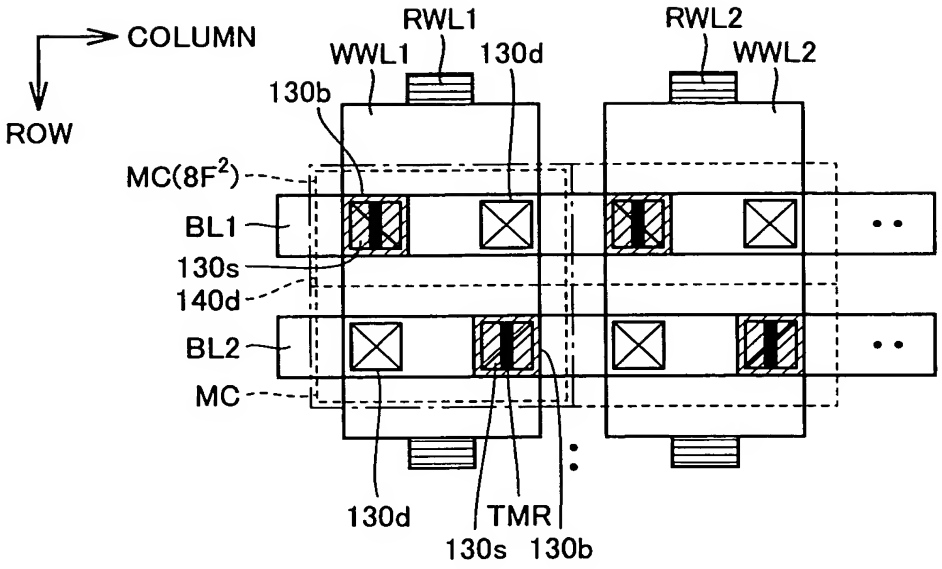
COLUMN
ROW
RWL1
WWL1
130d
RWL2
WWL2
130b
MC(8F2)
BL1
130s
140d
BL2
MC
130d
TMR
130s
130b

FIG.29

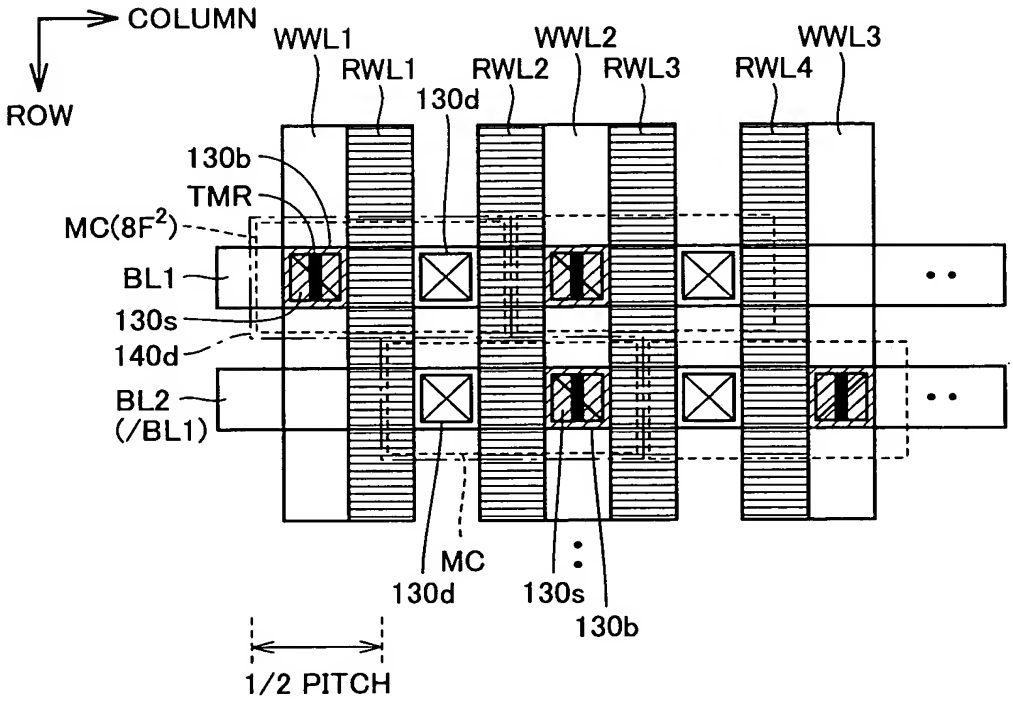
COLUMN
ROW
WWL1
RWL1
130d
WWL2
RWL2
RWL3
WWL3
RWL4
130b
TMR
MC(8F2)
BL1
130s
140d
BL2
(/BL1)
MC
130d
130s
130b
1/2 PITCH

FIG.30

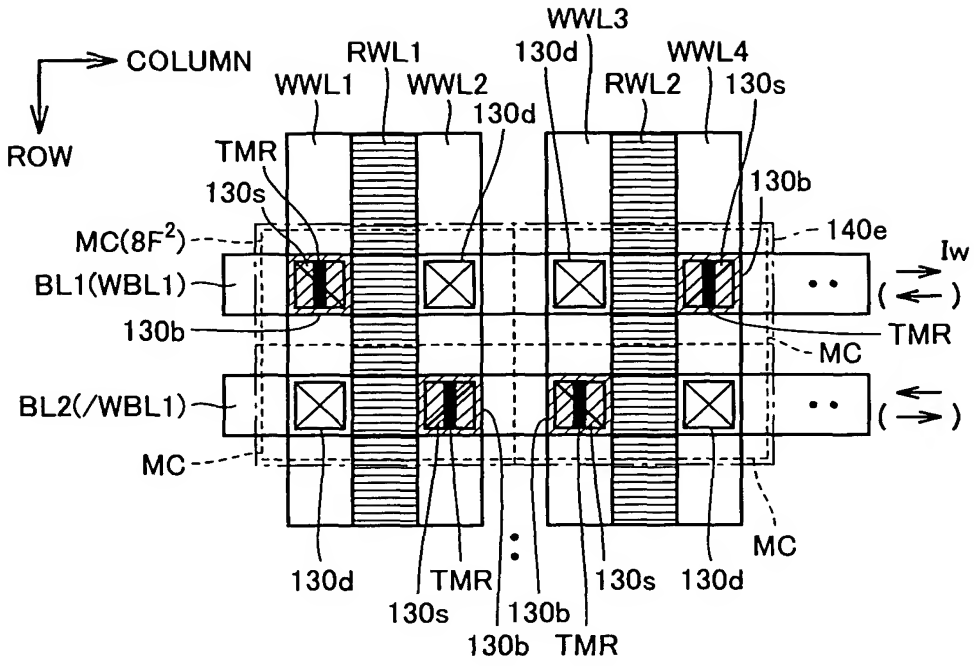

FIG.31

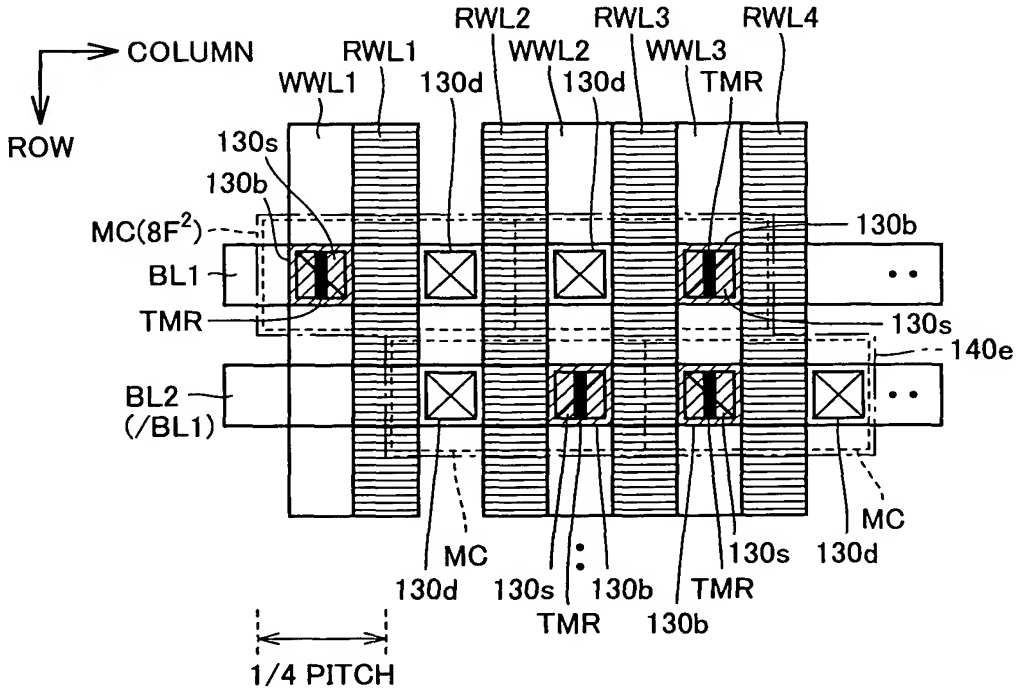

FIG.32

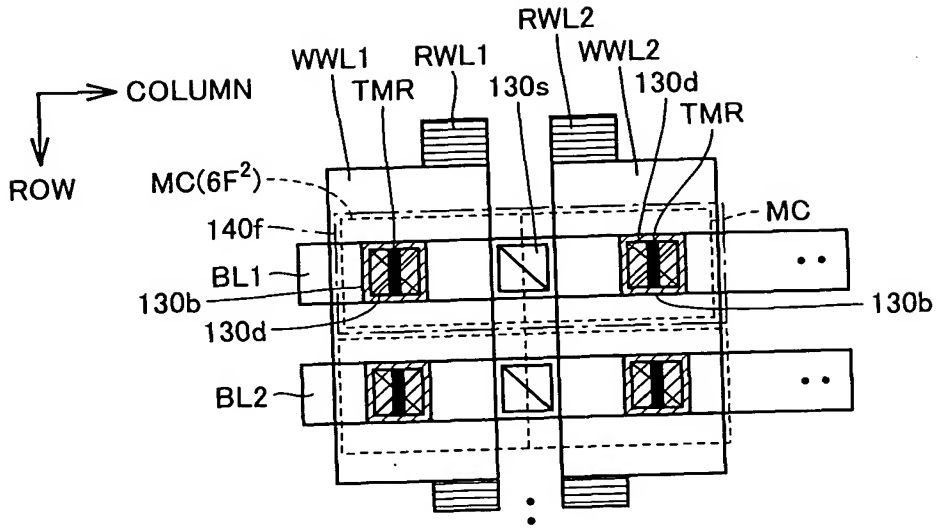

FIG.33

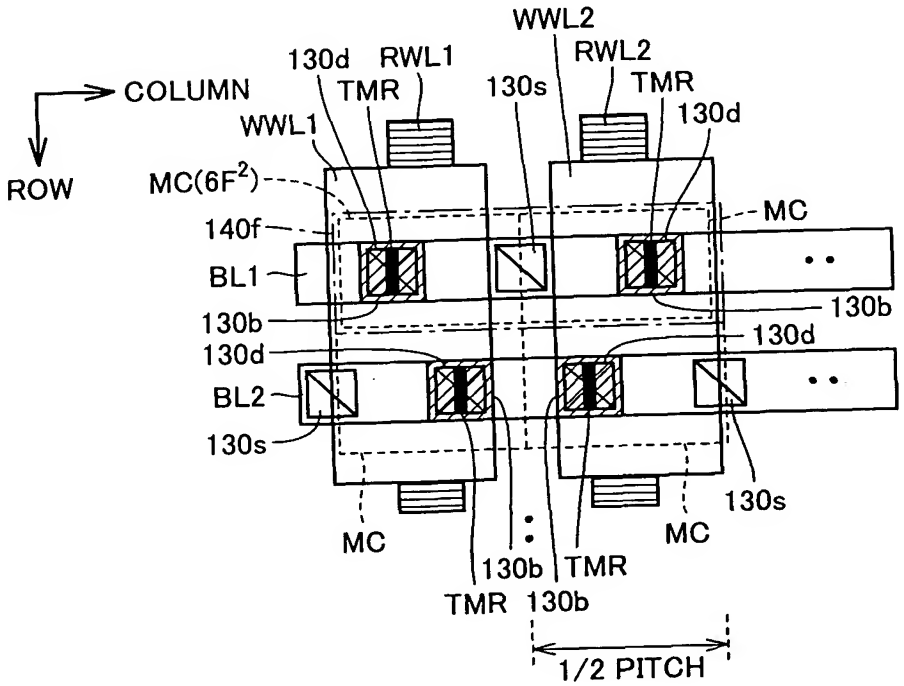

FIG.34

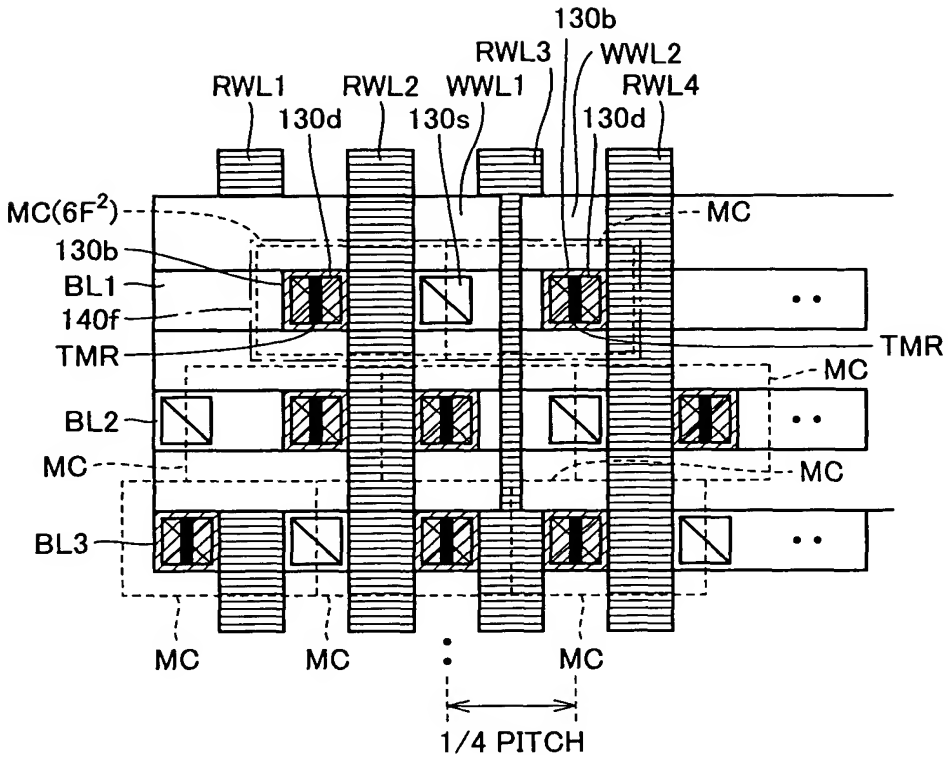
130b
RWL3
WWL2
RWL1
RWL2
WWL1
RWL4
130d
130s
130d
MC(6F2)
MC
130b
BL1
140f
TMR
TMR
MC
BL2
MC
MC
BL3
MC
MC
MC
1/4 PITCH

FIG.35

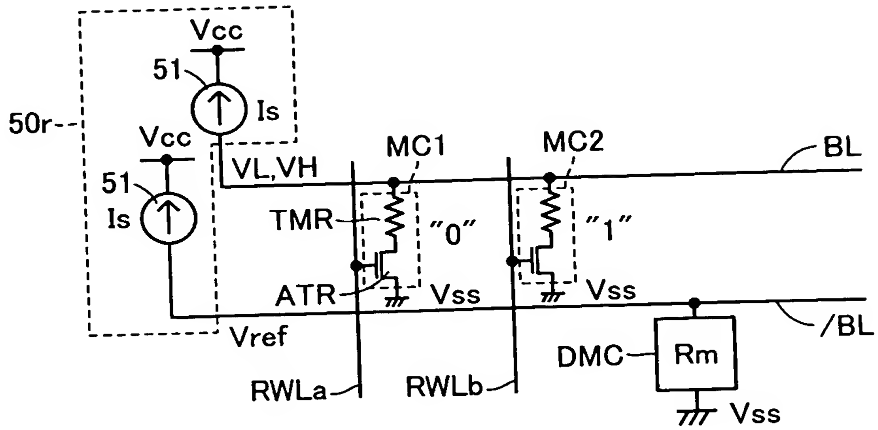

FIG.36

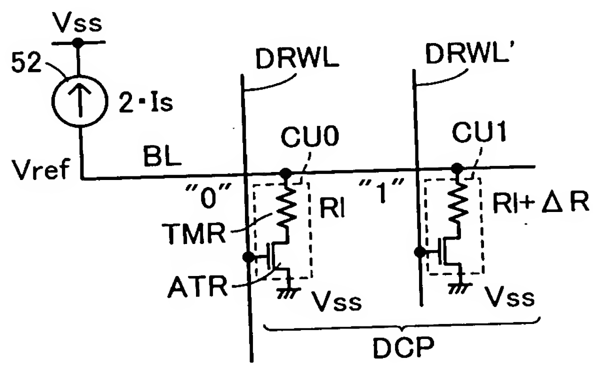

FIG.37

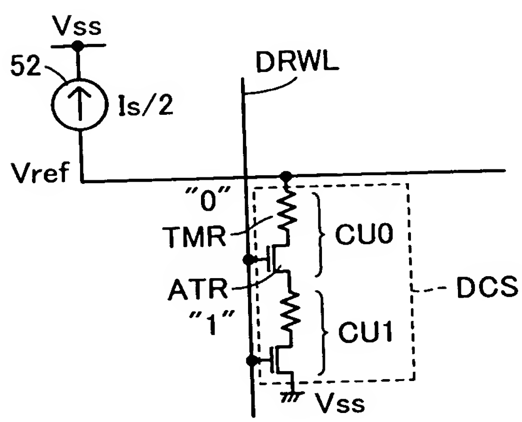

FIG.38

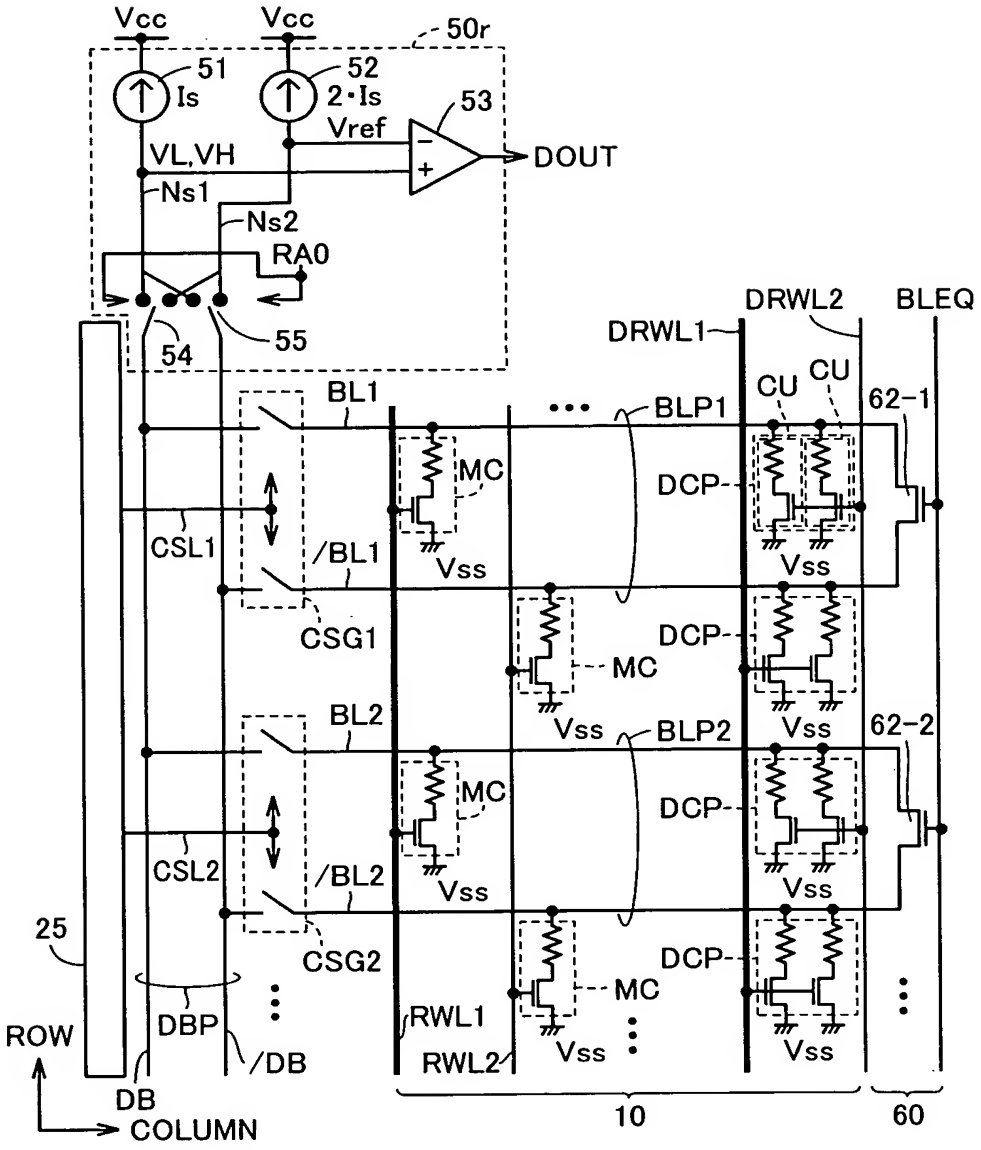
Vcc
Vcc
50r
51
Is
52
2·Is
53
Vref
VL,VH
DOUT
Ns1
Ns2
RA0
54
55
DRWL1
DRWL2
BLEQ
BL1
BLP1
CU
CU
62-1
MC
DCP-
CSL1
/BL1
Vss
CSG1
BL2
BLP2
62-2
CSL2
/BL2
CSG2
25
ROW
DBP
/DB
DB
COLUMN
RWL1
RWL2
10
60

FIG.39

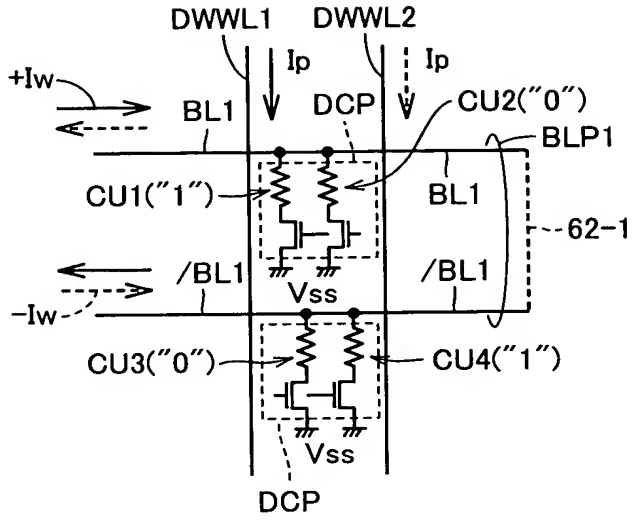

FIG.40

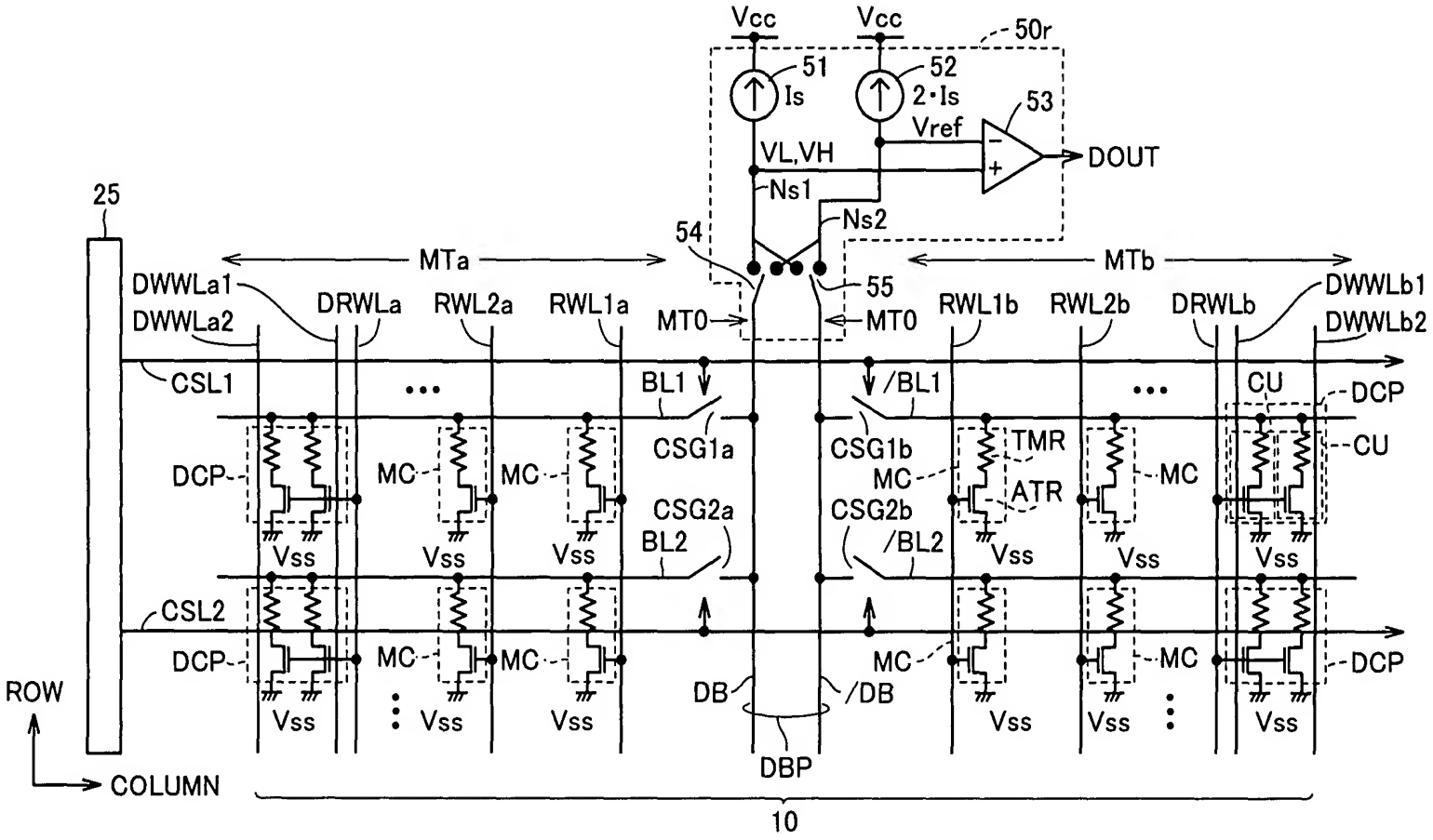
Vcc
Vcc
50r
51
Is
52
2·Is
53
Vref
VL,VH
DOUT
Ns1
Ns2
54
55
25
MTa
MTb
DWWLa1
DWWLa2
DRWLa
RWL2a
RWL1a
MT0
MT0
RWL1b
RWL2b
DRWLb
DWWLb1
DWWLb2
CSL1
BL1
/BL1
CU
DCP
CSG1a
CSG1b
TMR
MC
ATR
CSG2a
CSG2b
BL2
/BL2
Vss
CSL2
DB
/DB
DBP
ROW
COLUMN
10

FIG.41

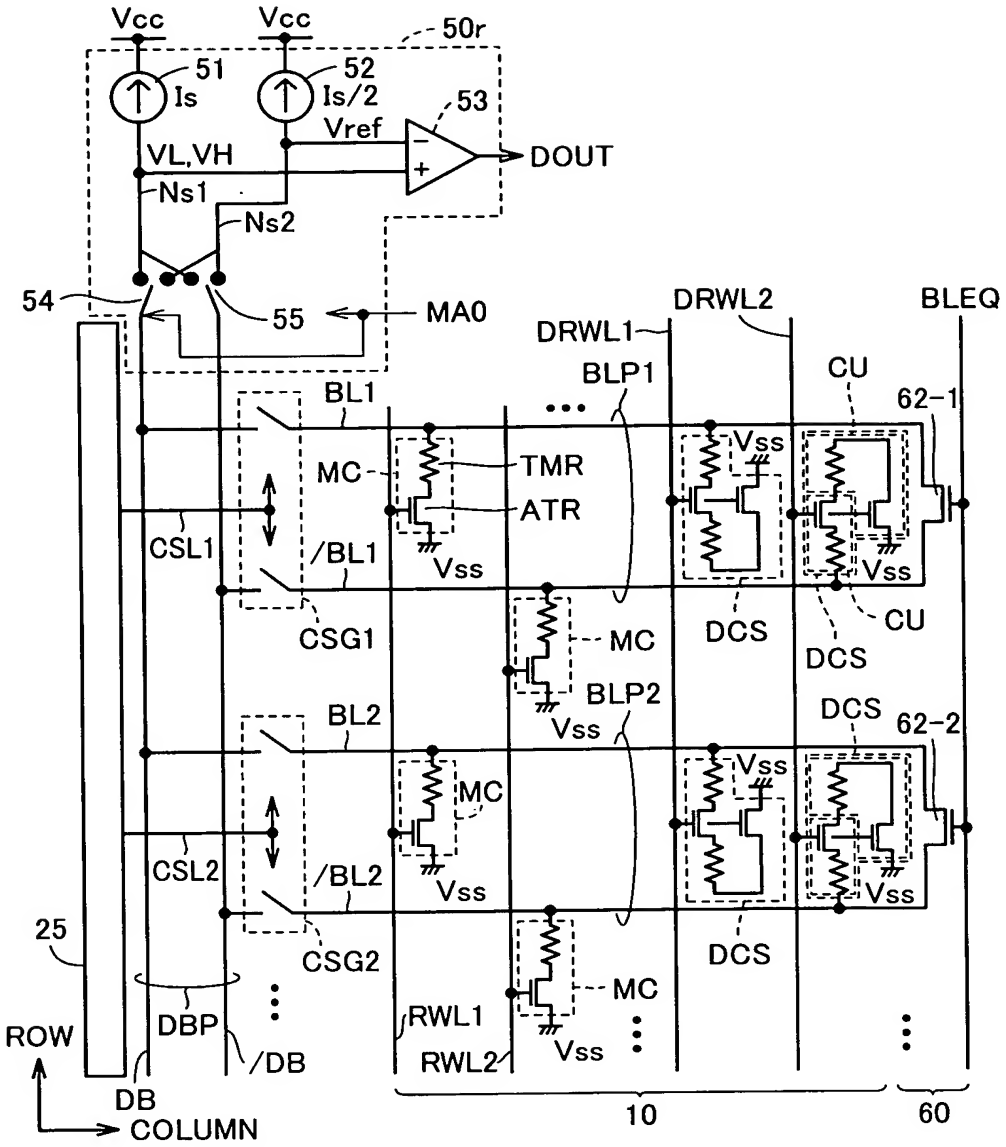
Vcc
Vcc
50r
51
Is
52
Is/2
53
Vref
VL,VH
DOUT
Ns1
Ns2
54
55
MA0
DRWL1
DRWL2
BLEQ
BLP1
CU
62-1
BL1
MC
TMR
ATR
Vss
CSL1
/BL1
CSG1
DCS
BLP2
BL2
62-2
CSL2
/BL2
CSG2
25
ROW
DBP
/DB
DB
COLUMN
RWL1
RWL2
10
60

FIG.42

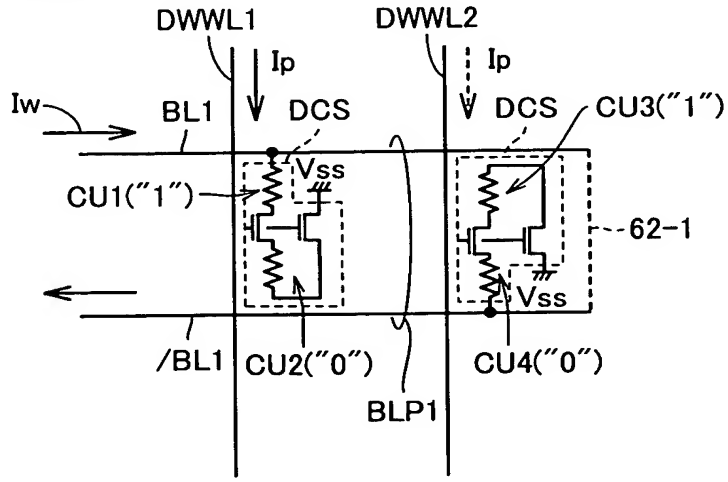
DWWL1
DWWL2
Ip
Iw
BL1
DCS
CU3("1")
Vss
CU1("1")
62-1
/BL1
CU2("0")
CU4("0")
BLP1

FIG.43

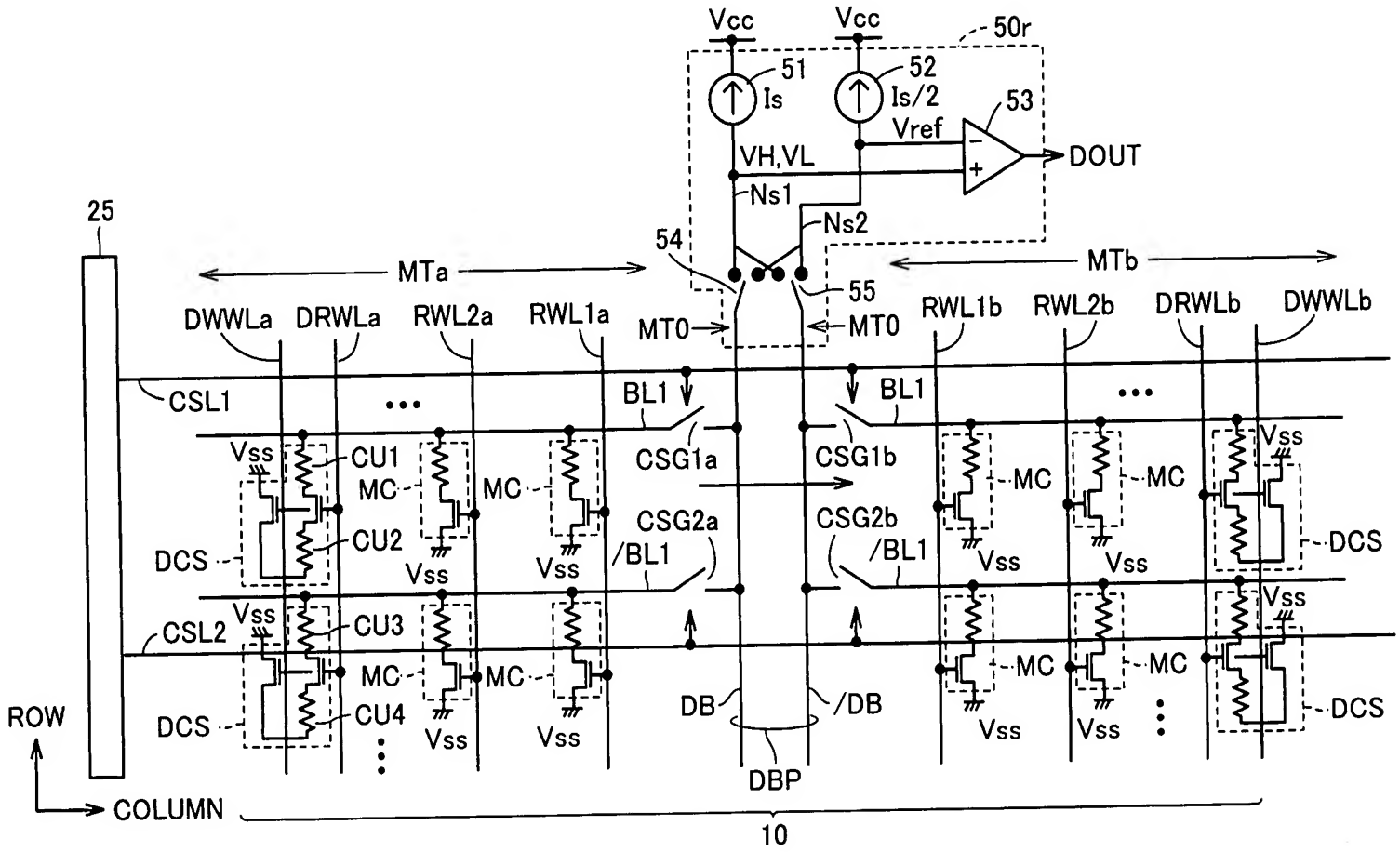
Vcc
Vcc
50r
51
Is
52
Is/2
53
Vref
VH,VL
DOUT
Ns1
Ns2
25
54
MTa
MTb
55
DWWLa
DRWLa
RWL2a
RWL1a
MT0
MT0
RWL1b
RWL2b
DRWLb
DWWLb
CSL1
BL1
BL1
Vss
CU1
MC
MC
CSG1a
CSG1b
MC
MC
Vss
CSG2a
CSG2b
DCS
CU2
/BL1
/BL1
DCS
Vss
Vss
Vss
Vss
Vss
CSL2
Vss
CU3
MC
MC
MC
MC
Vss
DB
/DB
DCS
CU4
DCS
Vss
Vss
Vss
Vss
ROW
DBP
COLUMN
10

FIG.44

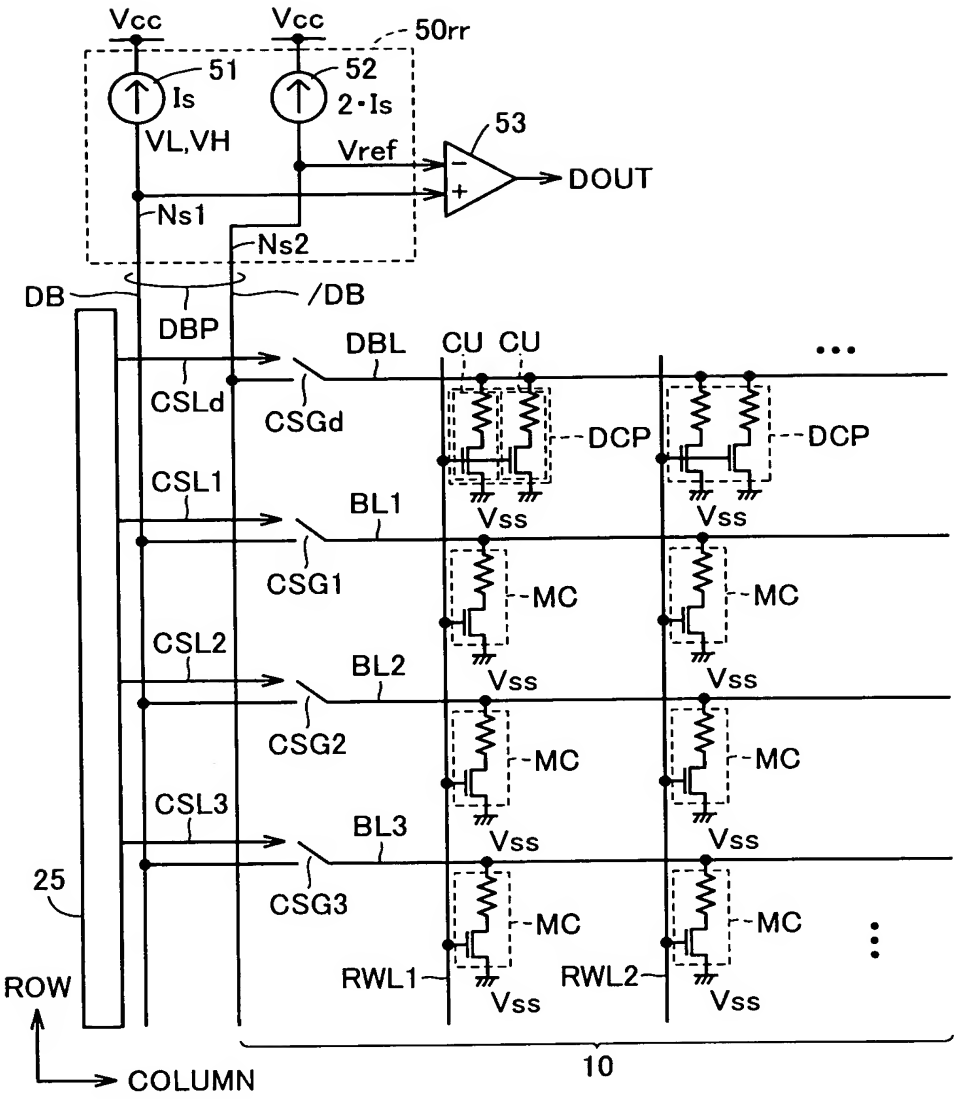
Vcc
Vcc
50rr
51
Is
52
2·Is
VL,VH
Vref
53
DOUT
Ns1
Ns2
DB
/DB
DBP
DBL
CU
CU
CSLd
CSGd
DCP
DCP
CSL1
BL1
CSG1
MC
MC
Vss
CSL2
BL2
CSG2
CSL3
BL3
CSG3
25
RWL1
RWL2
ROW
COLUMN
10

FIG.45

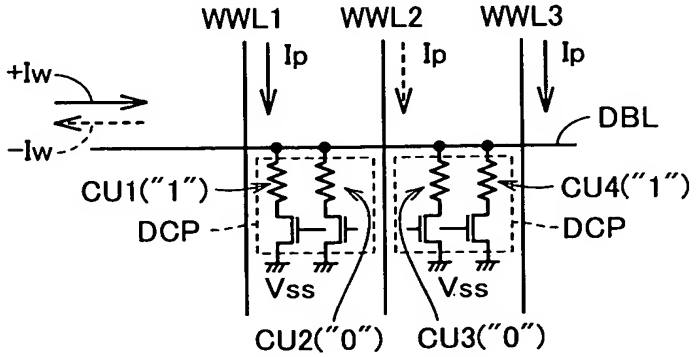
WWL1
WWL2
WWL3
Ip
Ip
Ip
+Iw
-Iw
DBL
CU1("1")
CU4("1")
DCP
DCP
Vss
Vss
CU2("0")
CU3("0")

FIG.46

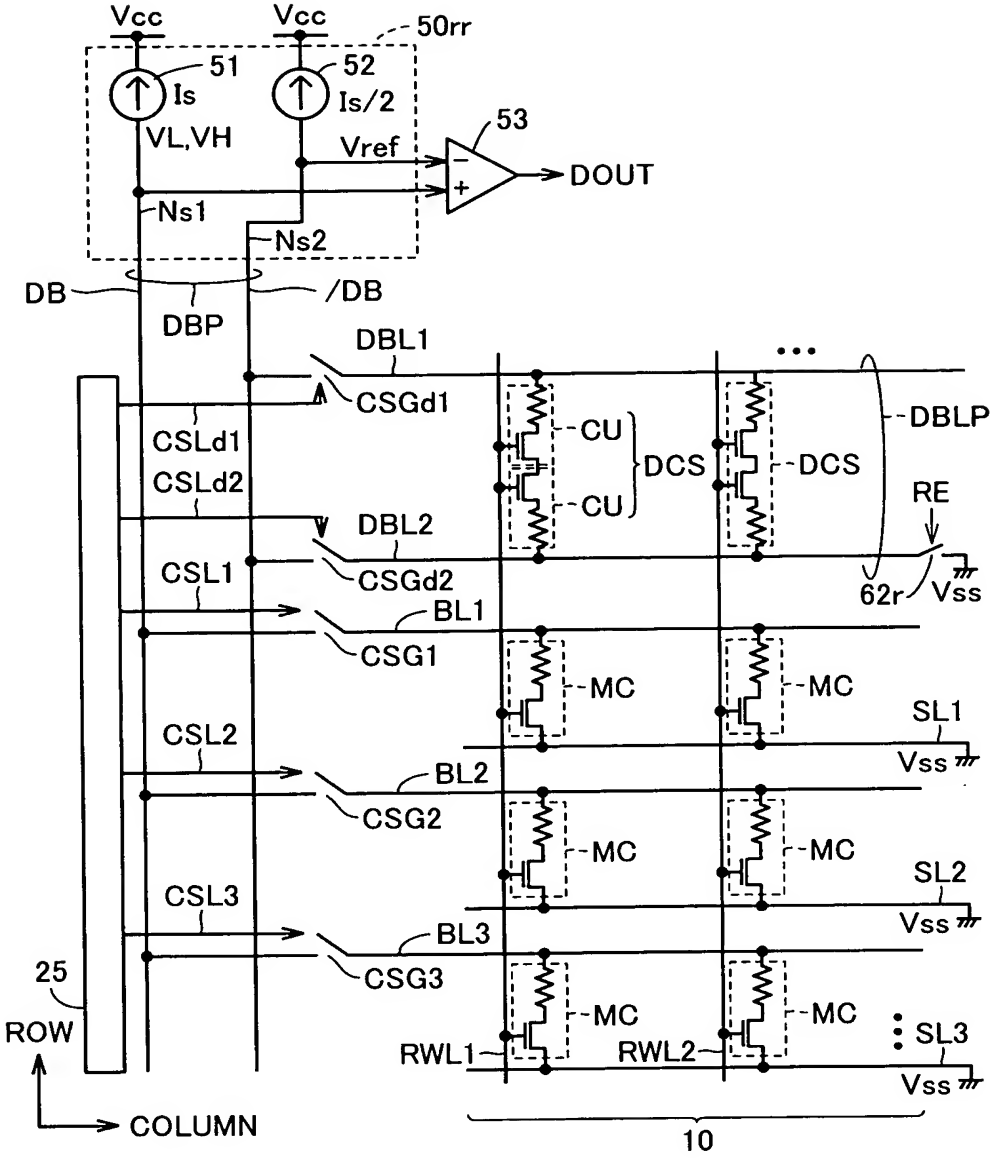
Vcc
Vcc
50rr
51
Is
52
Is/2
VL,VH
Vref
53
DOUT
Ns1
Ns2
DB
/DB
DBP
DBL1
CSGd1
CSLd1
CSLd2
CU
CU
DCS
DCS
DBLP
RE
DBL2
CSGd2
CSL1
62r
Vss
BL1
CSG1
MC
MC
SL1
CSL2
Vss
BL2
CSG2
MC
MC
SL2
CSL3
Vss
BL3
CSG3
25
MC
MC
SL3
ROW
RWL1
RWL2
Vss
COLUMN
10

FIG.47

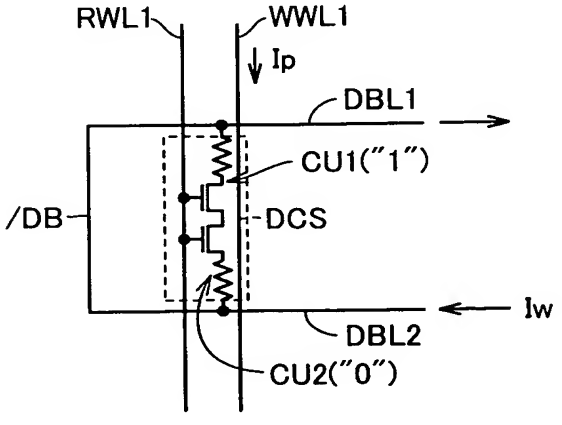
RWL1
WWL1
Ip
DBL1
CU1("1")
/DB
DCS
Iw
DBL2
CU2("0")

FIG.48

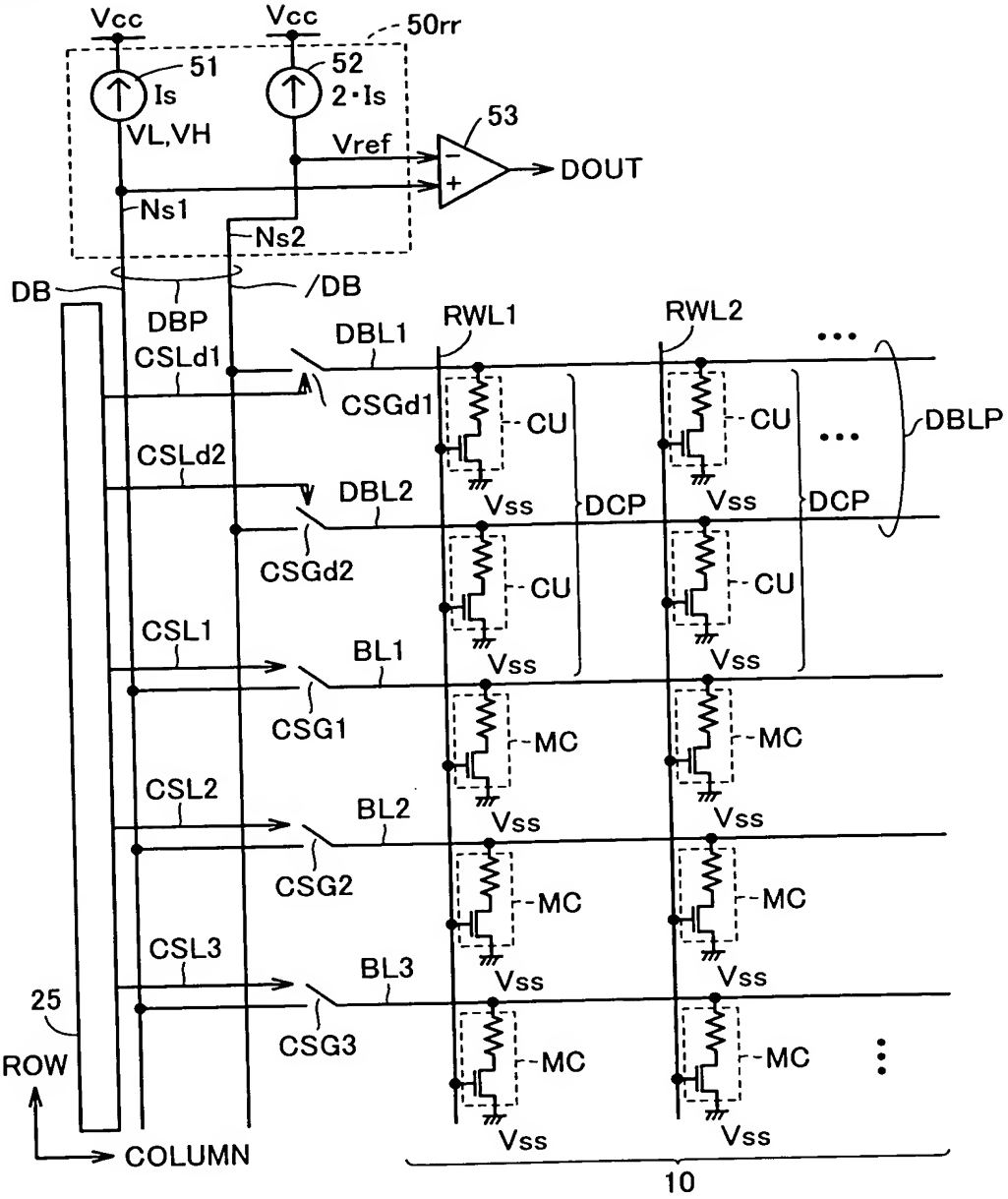

FIG.49

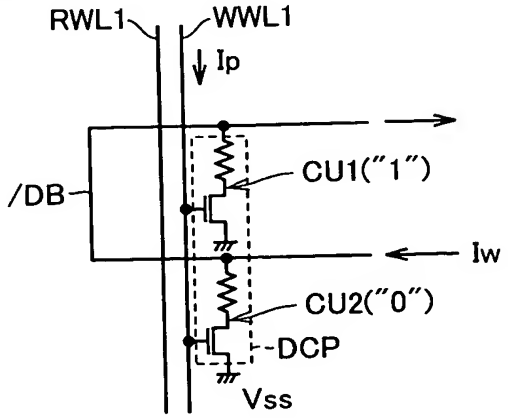

FIG.50A

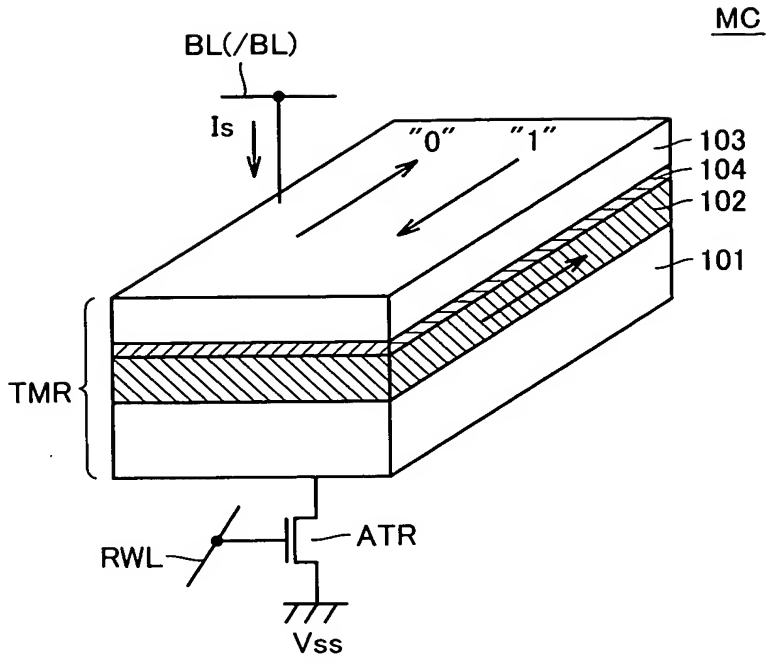

FIG.50B

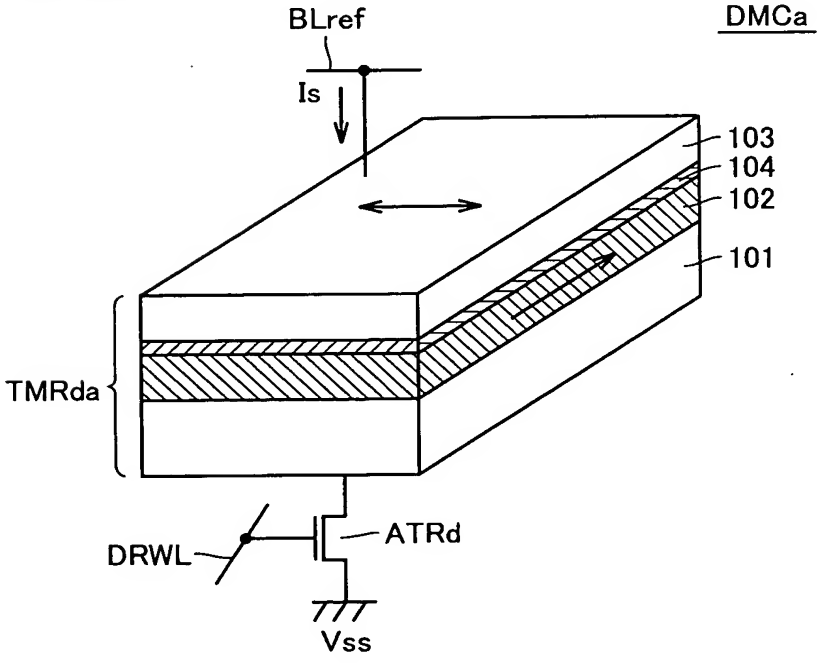

FIG.51

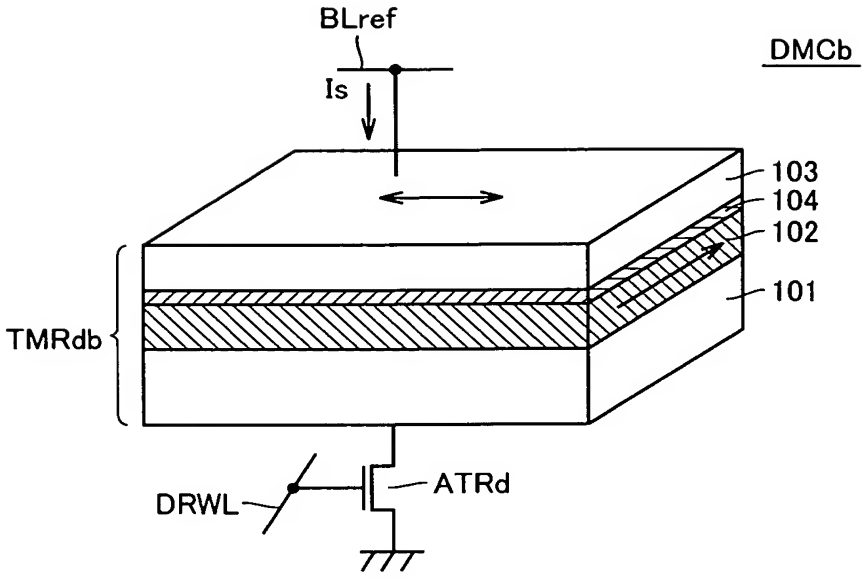

FIG.52

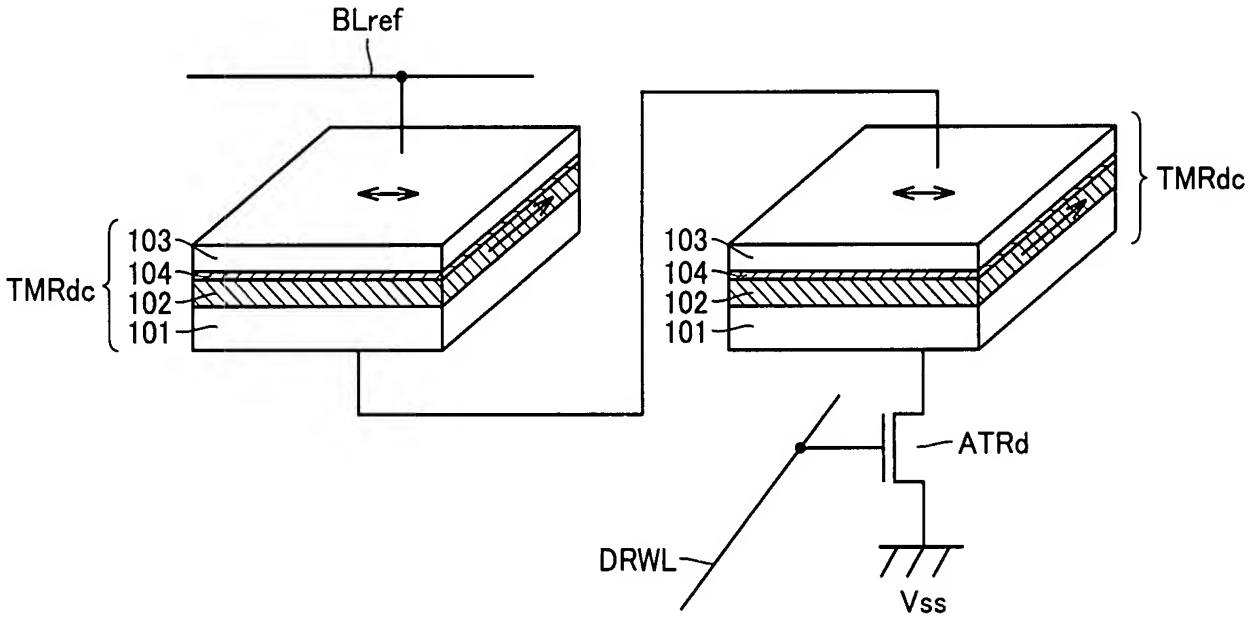
BLref
TMRdc
103
104
102
101
TMRdc
103
104
102
101
TMRdc
ATRd
DRWL
Vss

FIG.53

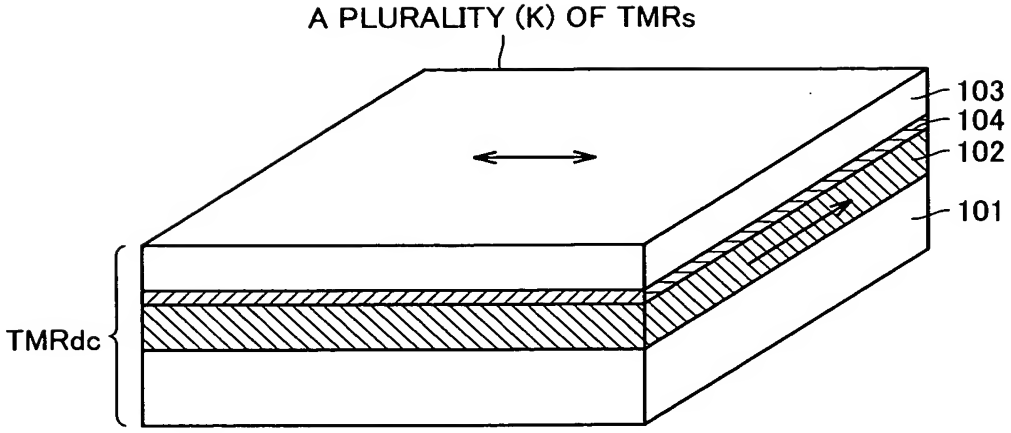
A PLURALITY (K) OF TMRs
103
104
102
101
TMRdc

FIG.54

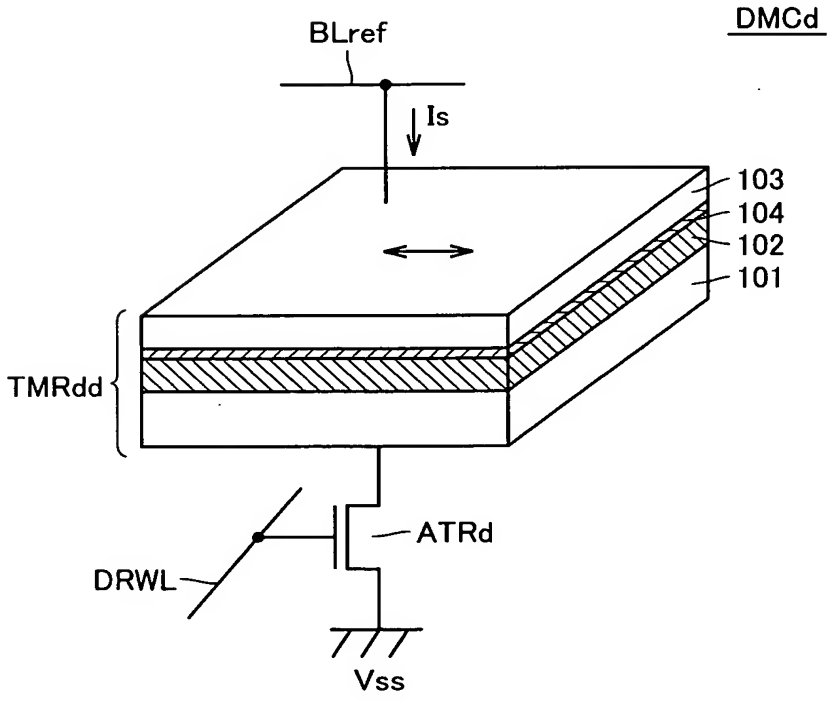
DMCd
BLref
Is
103
104
102
101
TMRdd
ATRd
DRWL
Vss

FIG.55

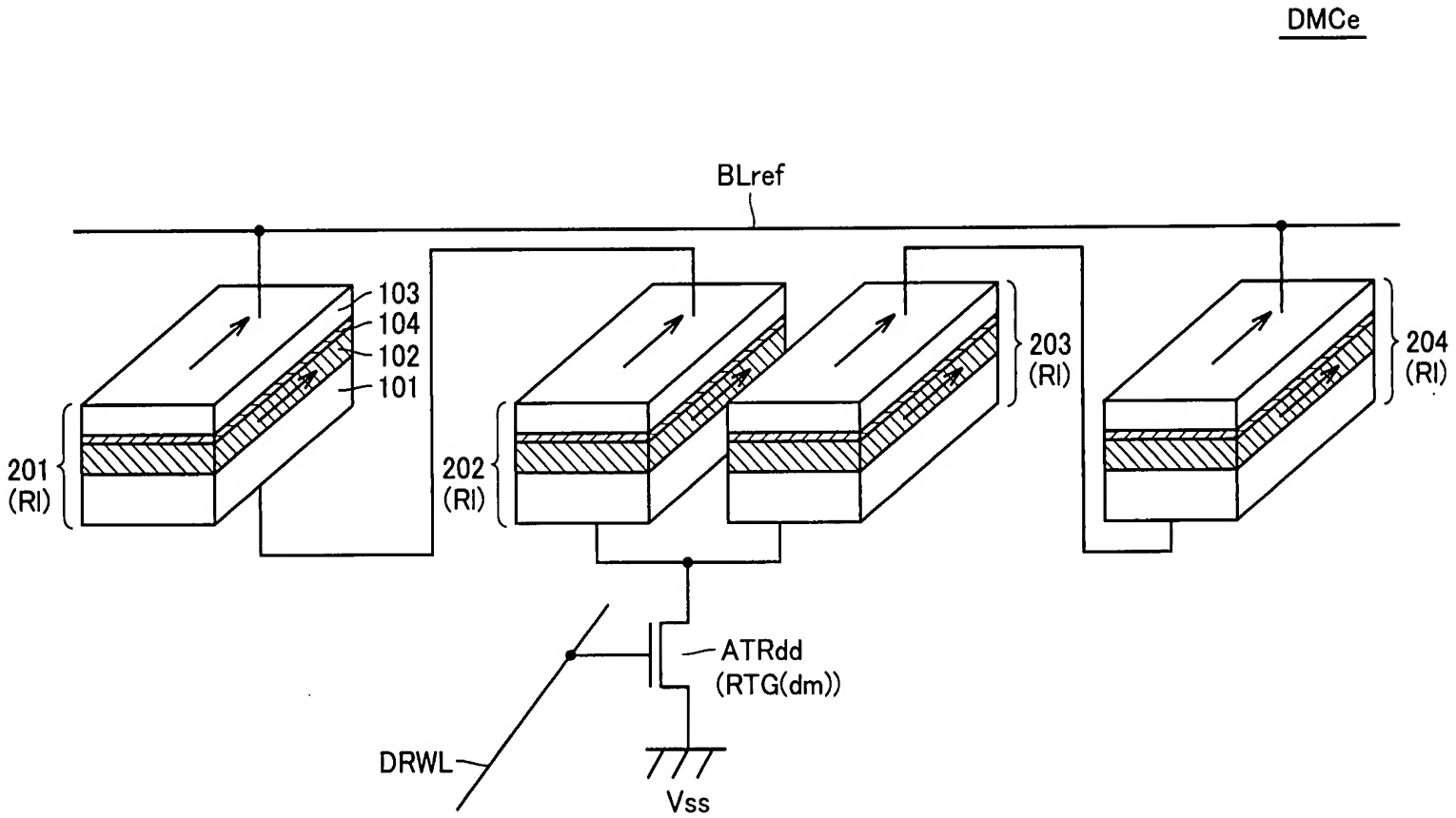
DMCe
BLref
103
104
102
101
201
(RI)
202
(RI)
203
(RI)
204
(RI)
ATRdd
(RTG(dm))
DRWL
Vss

FIG.56

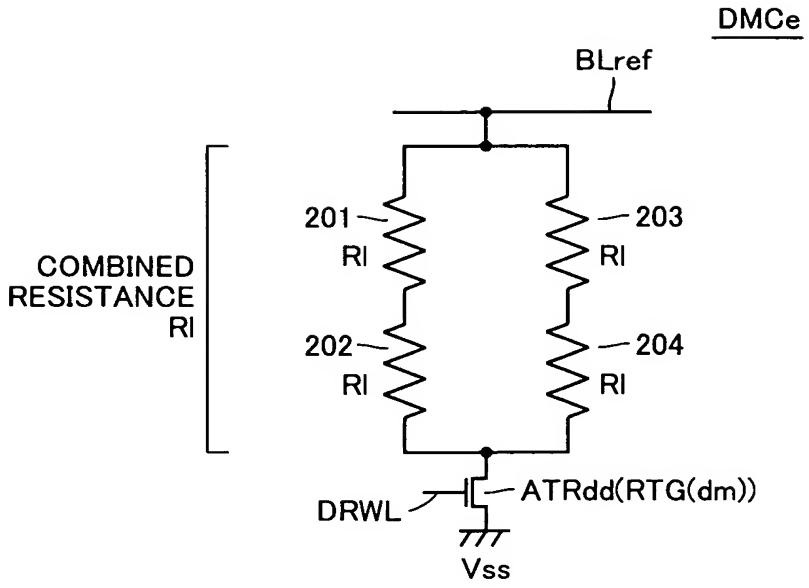
DMCe
BLref
COMBINED
RESISTANCE
RI
201
RI
202
RI
203
RI
204
RI
DRWL
ATRdd(RTG(dm))
Vss

FIG.57

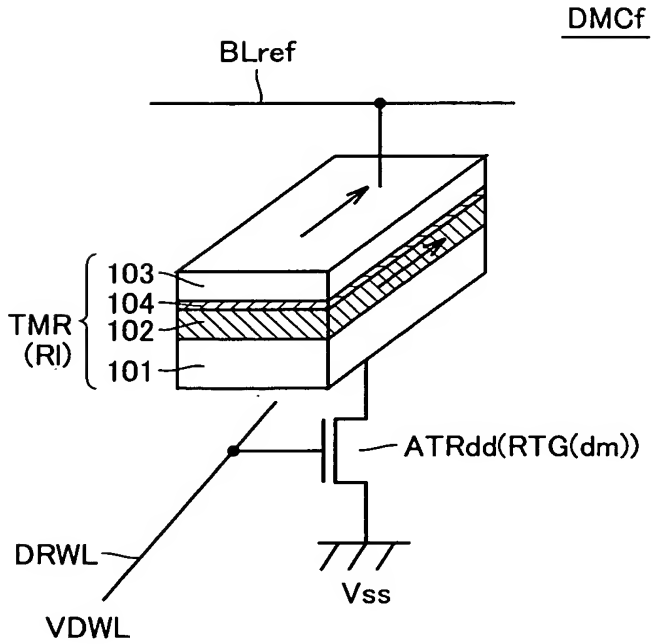
DMCf
BLref
TMR
(RI)
103
104
102
101
ATRdd(RTG(dm))
DRWL
VDWL
Vss

FIG.58

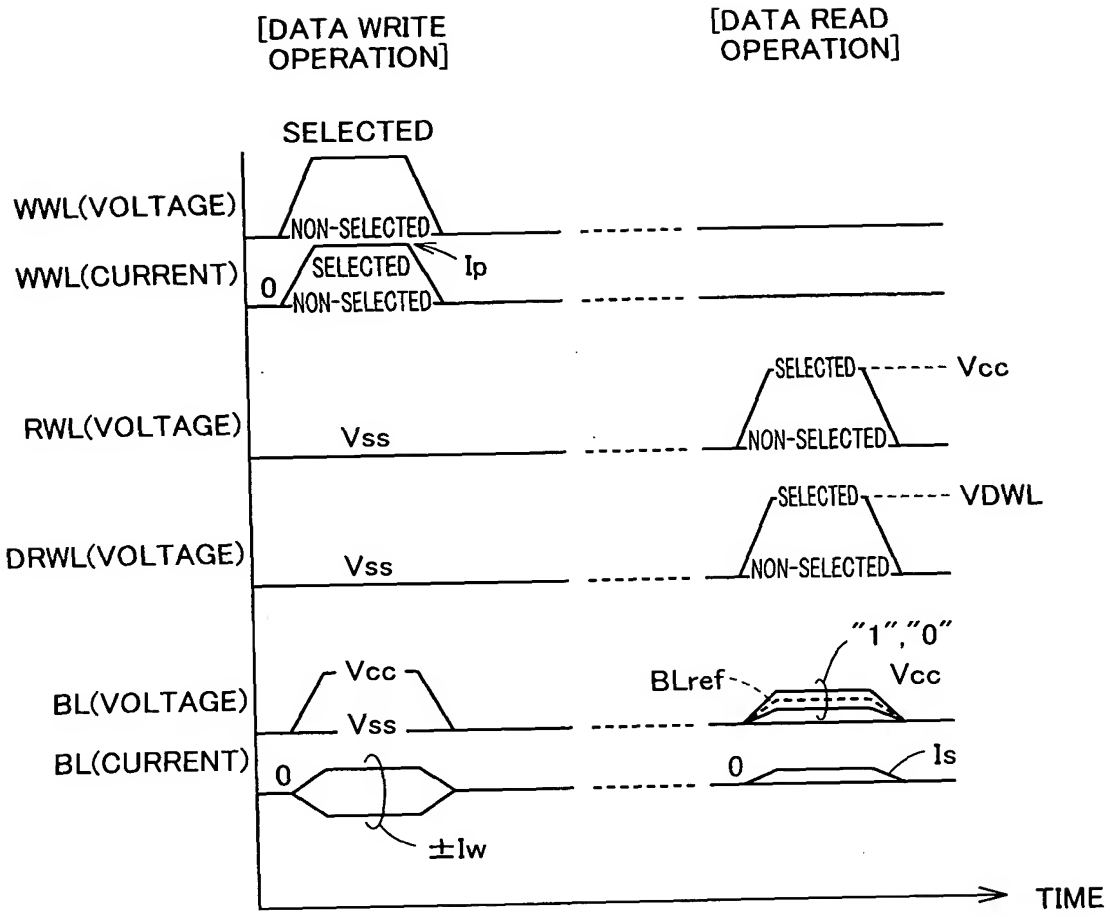
[DATA WRITE OPERATION]
[DATA READ OPERATION]
SELECTED
WWL(VOLTAGE)
NON-SELECTED
WWL(CURRENT)
0
SELECTED
NON-SELECTED
Ip
RWL(VOLTAGE)
Vss
SELECTED
Vcc
NON-SELECTED
DRWL(VOLTAGE)
Vss
SELECTED
VDWL
NON-SELECTED
BL(VOLTAGE)
Vcc
Vss
BLref
"1","0"
Vcc
BL(CURRENT)
0
±Iw
0
Is
TIME

FIG.59

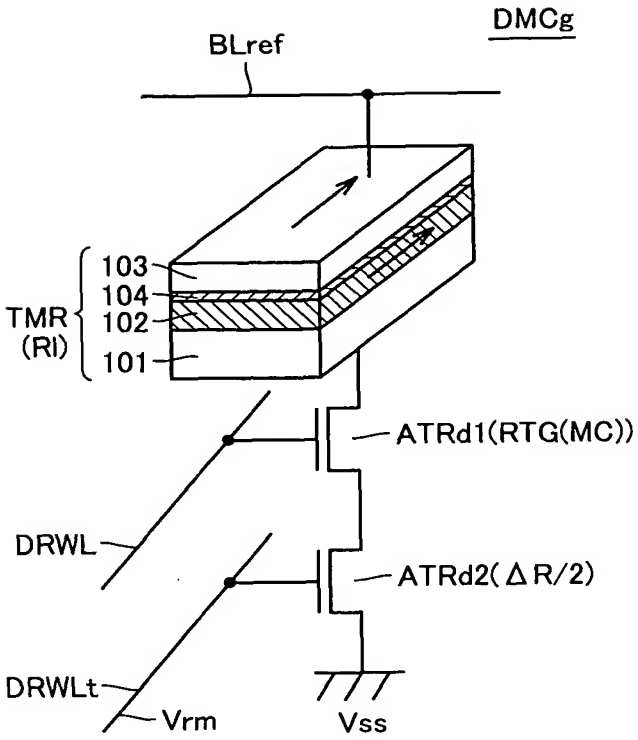

FIG.60

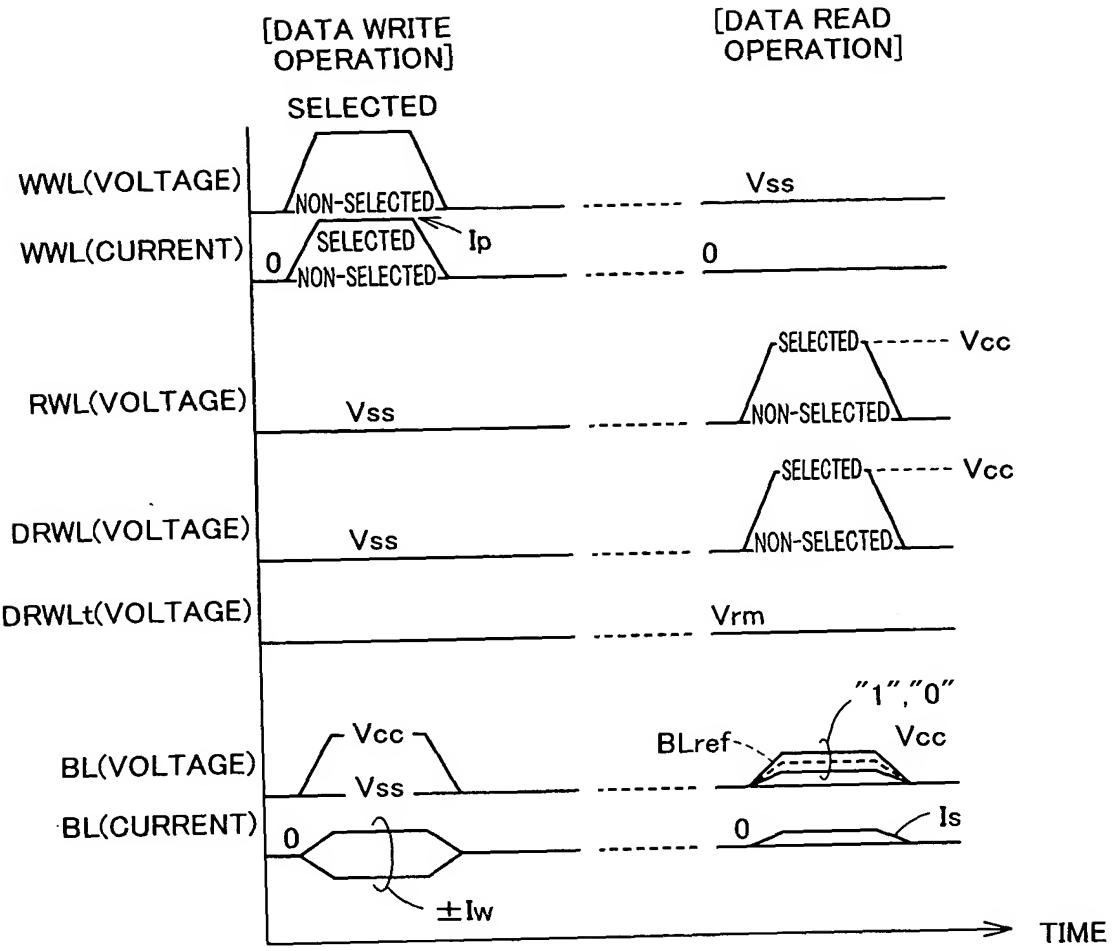
[DATA WRITE OPERATION]
[DATA READ OPERATION]
SELECTED
WWL(VOLTAGE)
NON-SELECTED
Vss
WWL(CURRENT)
SELECTED
Ip
0
NON-SELECTED
0
SELECTED
Vcc
RWL(VOLTAGE)
Vss
NON-SELECTED
SELECTED
Vcc
DRWL(VOLTAGE)
Vss
NON-SELECTED
DRWLt(VOLTAGE)
Vrm
"1","0"
Vcc
BLref
BL(VOLTAGE)
Vcc
Vss
BL(CURRENT)
0
0
Is
±Iw
TIME

FIG.61

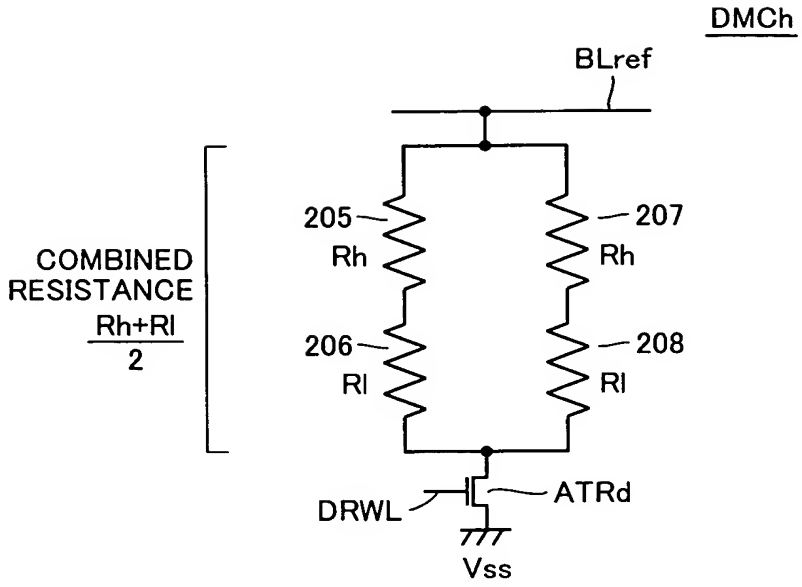

FIG.62

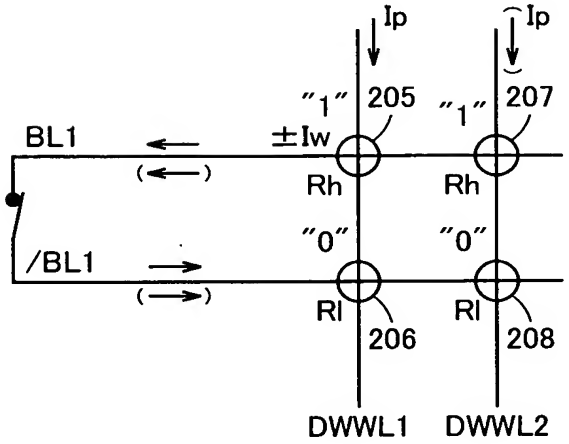

FIG.63

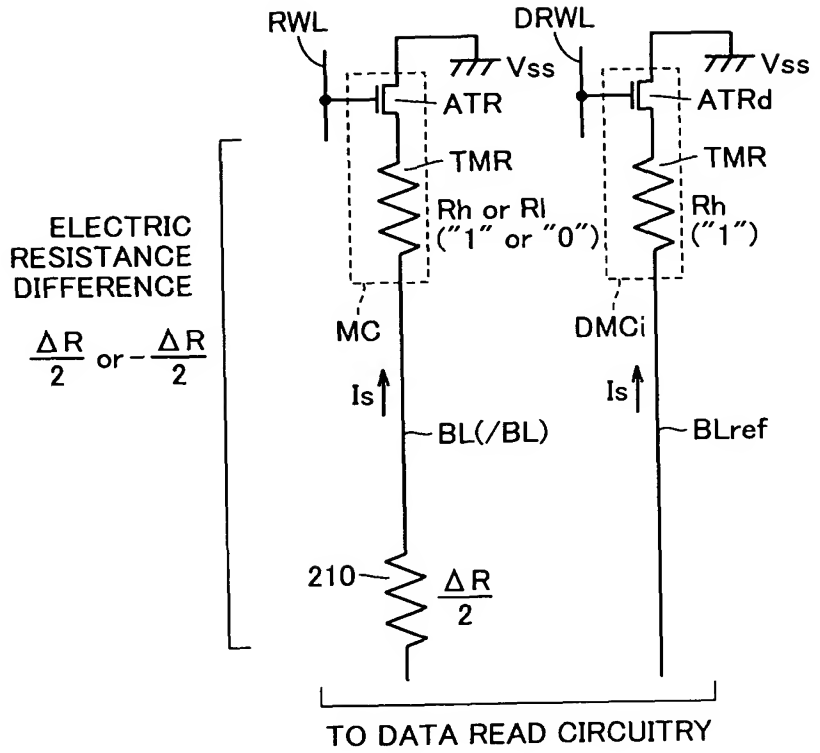
RWL
DRWL
Vss
Vss
ATR
ATRd
TMR
TMR
Rh or Rl
("1" or "0")
Rh
("1")
ELECTRIC
RESISTANCE
DIFFERENCE
ΔR/2 or -ΔR/2
MC
DMCi
Is
Is
BL(/BL)
BLref
210
ΔR/2
TO DATA READ CIRCUITRY

FIG.64

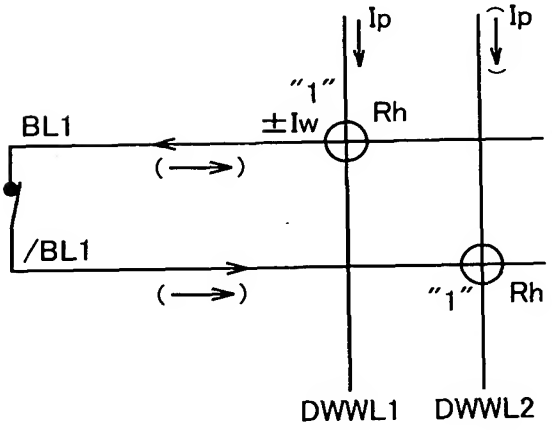
Ip
Ip
"1"
±Iw
Rh
BL1
/BL1
"1"
Rh
DWWL1
DWWL2

FIG.65

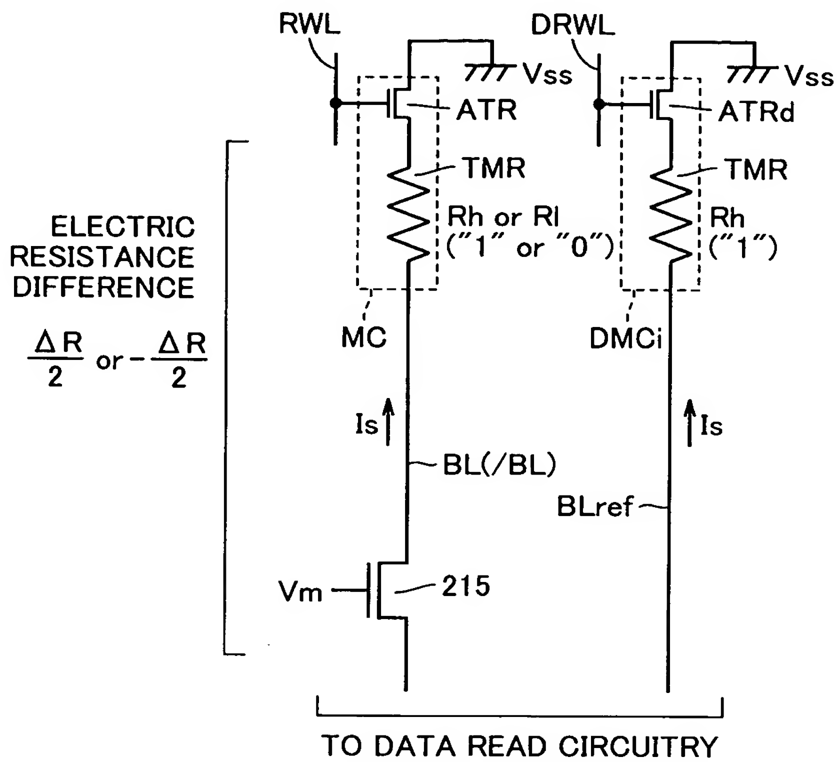
RWL
DRWL
Vss
Vss
ATR
ATRd
TMR
TMR
Rh or Rl
("1" or "0")
Rh
("1")
ELECTRIC
RESISTANCE
DIFFERENCE
ΔR/2 or −ΔR/2
MC
DMCi
Is
Is
BL(/BL)
BLref
Vm
215
TO DATA READ CIRCUITRY

FIG.66 PRIOR ART

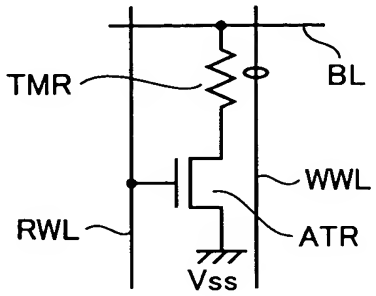

FIG.67 PRIOR ART

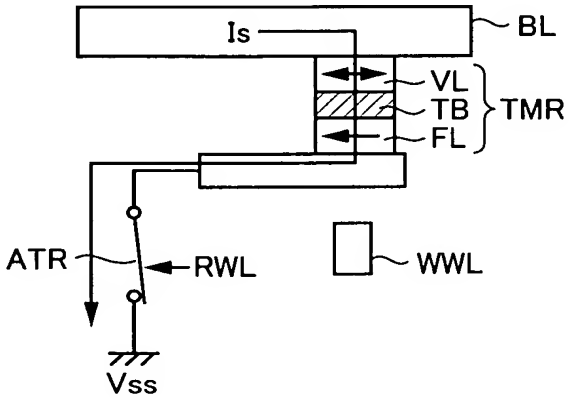

FIG.68 PRIOR ART

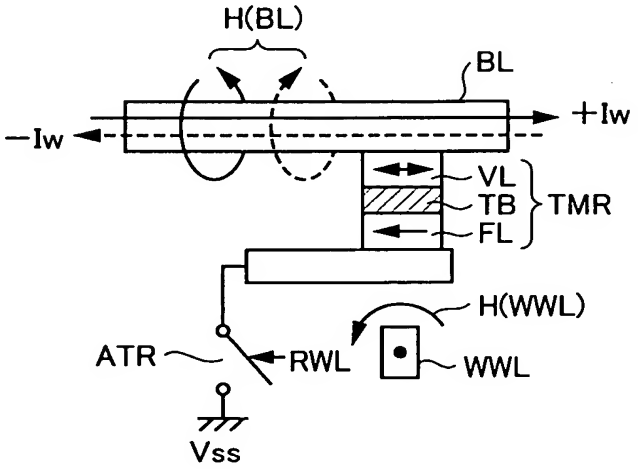

FIG.69 PRIOR ART